

**SEMICONDUCTOR MEMORY**

**DESIGN**

**SAMSUNG 128K x 8 Low power, Low voltage SRAM (K6X1008T2D)**



**SUBMITTED BY:**

BHARATH NANDAKUMAR

JAHNAVI KULKARNI

PRATEEK JAIN

ROHIT JEEVNANI

INDIAN INSTITUTE OF TECHNOLOGY DELHI

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**1. Features**

|  |  |  |
| --- | --- | --- |
| **Memory Type** | SRAM |  |
|  |
|  |  |  |
| **Memory Size** | 128k x 8 bits |  |
|  |
|  |  |  |
| **Data Width** | 8 bit |  |
|  |
|  |  |  |
| **Address Width** | 17 bit |  |
|  |
|  |  |  |
| **Operating Voltage** | 1 V |  |
|  |
|  |  |  |
| **Cycle Time** | 85 ns |  |
|  |
|  |  |  |
| **Process Type With Feature Size** | Umc90nm |  |
|  |
|  |  |  |
| **No Of Metals** | 9 Metals used |  |
|  |
|  |  |  |
| **No Of Polys** |  |  |
| 1 |  |
|  |  |  |
| **Cell Size** | 2.44 um2 |  |
|  |
|  |  |  |
| **Core Efficiency** | 71% |  |
|  |
|  |  |  |
| **Logic** | Static, optimized pass |  |
|  |
|  | transistor logic |  |
| **Sense Amp Type** | Voltage mode |  |
|  |
|  |  |  |
| **Decoding Style** | Hierarchical |  |
|  |
|  |  |  |
| **No Of ATDs** | 1 |  |
|  |
|  |  |  |

1. **Background Information**
   1. PROCESS TECHNOLOGY

This memory is designed at 90nm technology node. At this node, minimum length and width of a transistor are 120nm and 80nm respectively. There are three types of transistors available in this technology – HSL (High Speed Logic), LLL (Low leakage logic) and SP(Standard Process). In this project High VT transistors N\_10\_SPHVT and P\_12\_SPHVT were used to achieve low leakage current and effectively low static power dissipation. High VT will also results in high noise margin.

**Device Model**

For SP transistors, some of the parameters are

Threshold of N\_10\_SPHVT: 0.305 V

Threshold of P\_10\_SPHVT: 0.379 V

Gate capacitance of Minimum sized NMOS: 0.2 fF (approx.)

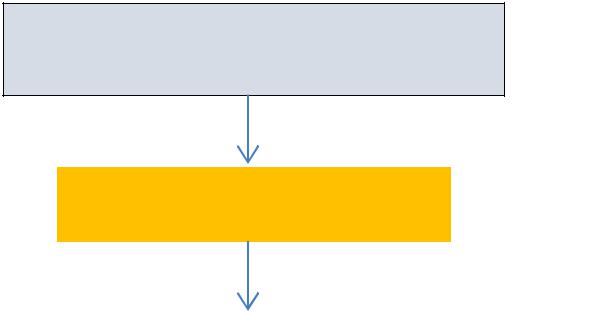
Drain capacitance of Minimum sized NMOS: 0.2 fF (approx.)

**Spice Control Parameter**

Relative Tolerance: 1e-3

V Absolute Tolerance: 1e-6

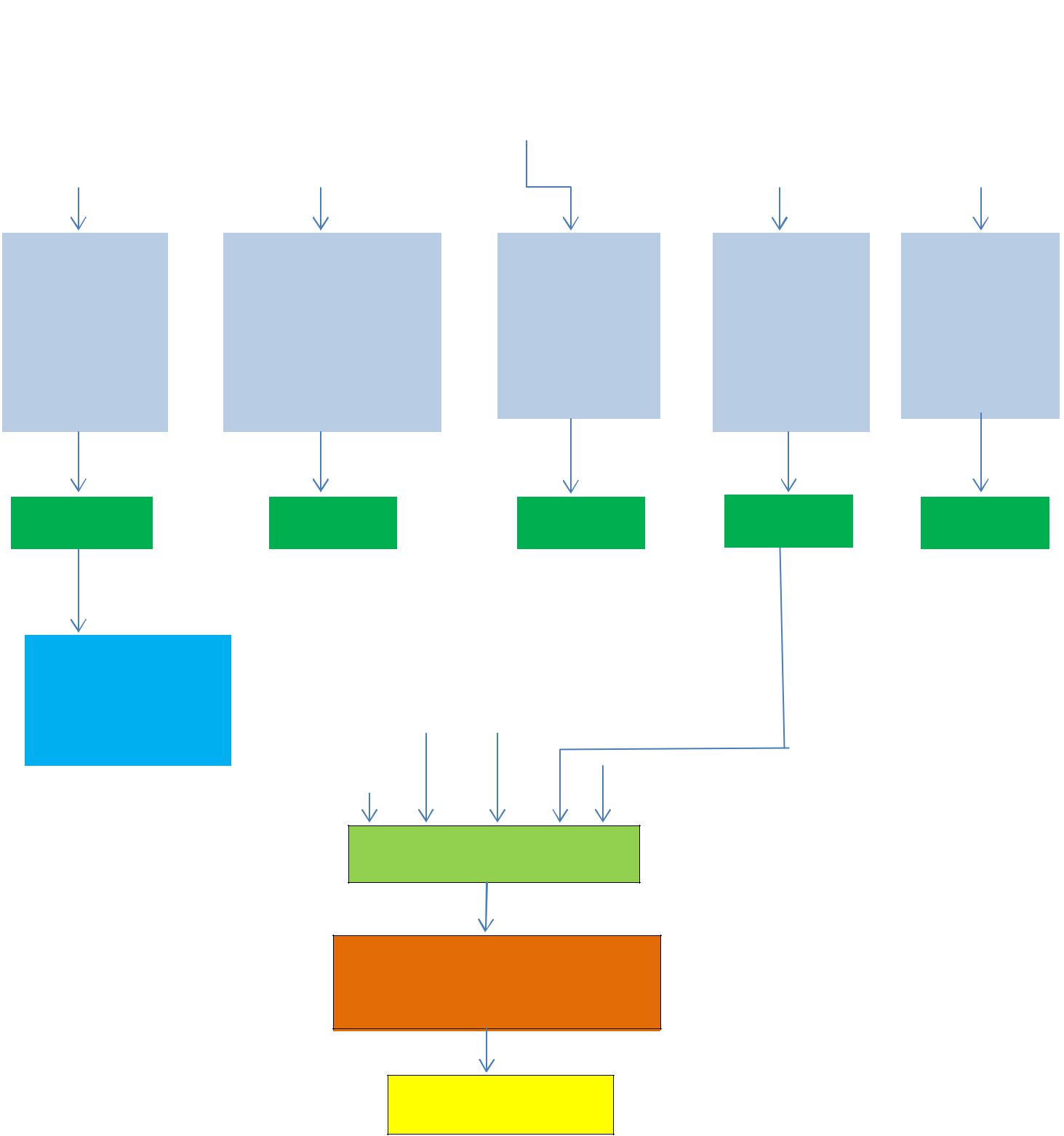
2.2 DESIGN FLOW DIAGRAM



**Finalizing the Specification** **s**



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **Architecture** | | | | | | | | |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **Floorplan** | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  | **SRAM Cell** | | | |  |  | **Row Decoder,** | | | | | | |  |  |  | **Sense** | | | | |  | |  | **Different** | |  |  | **ATD** | |  |  |
|  | **Design (CR,** | | | | |  |  |  | **Column** | | | | | |  |  | **Amplifier** | | | | | |  | |  | **Precharge** | |  |  | **Timing** | |  |  |
|  |  | **PR, SNM ,** | | | |  |  | **Decoder and** | | | | | | |  | **and Buffer** | | | | | | |  | |  | **Circuit** | |  |  | **Control** | |  |  |
|  |  | **Retention** | | | |  |  | **Process Corner** | | | | | | |  |  |  | **Design** | | | | |  | |  | **Topology** | |  |  | **Circuit** | |  |  |
|  |  | **voltage)** | | | |  |  | **Simulations** | | | | | | |  |  |  |  |  |  |  |  |  |  |  | **Analysis** | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  | **LAYOUT** | | |  | |  |  | **LAYOUT** | | | |  |  |  |  |  | **LAYOUT** | | | |  |  |  |  | **LAYOUT** |  |  |  | **LAYOUT** | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  | **Memory Block** | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **Integration** | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | **Layout** | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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**System Integration**

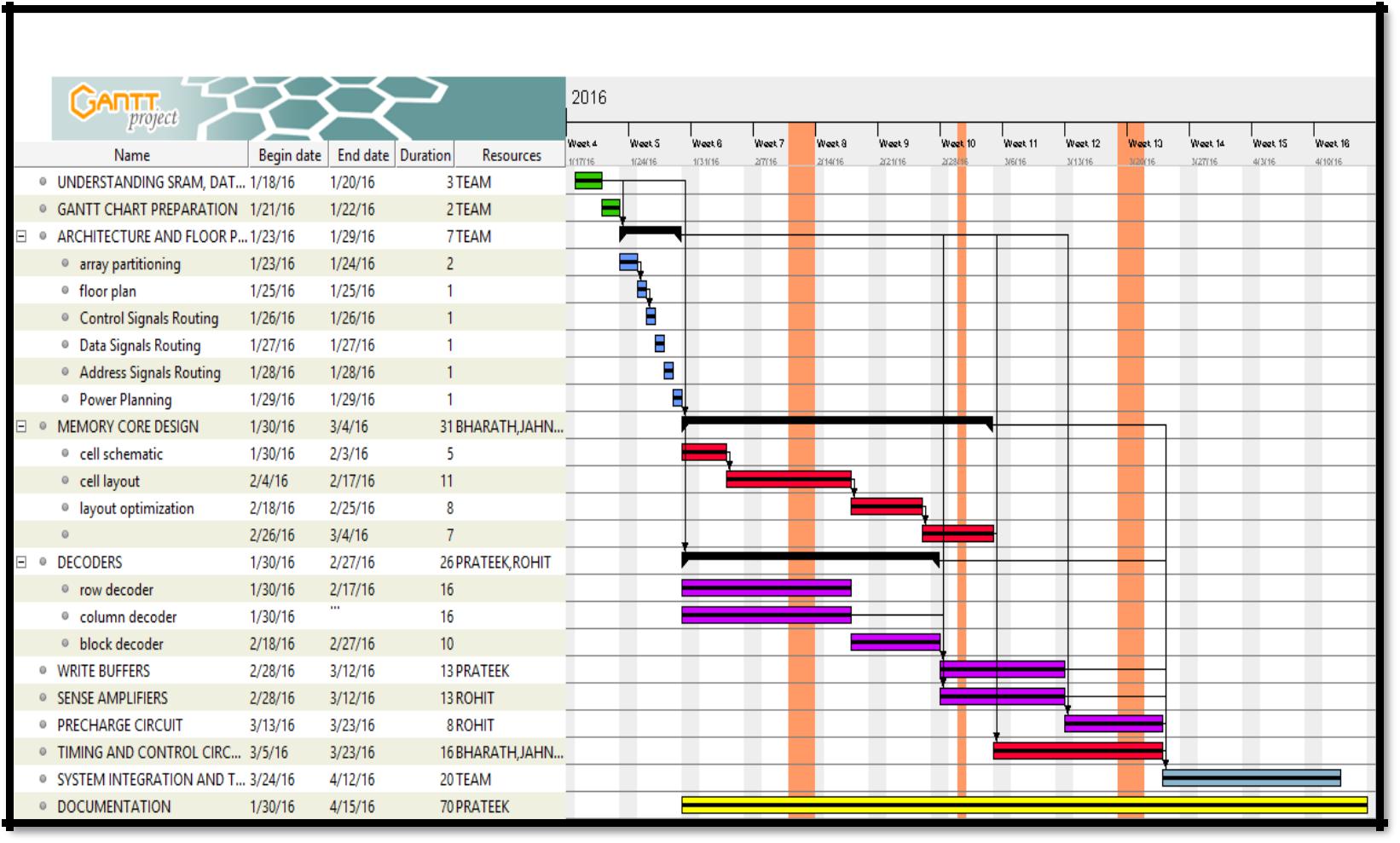
**Critical Path Simulation**

**and other Simulation**

**Documentation**

2.3 GANTT PROJECT

Gantt chart shows resource and time allocation for the completion of a project by four members over a period of 4 months. It helps us keep track of our progress.



**Figure 1: GANNT Chart**

1. LITERATURE SURVEY
   1. J.M.Rabaey, A.Chandrakasan, B.Nikolic, “*Digital Integrated Circuits: A Design Perspective*”

Prentice Hall

* 1. IBM Application Note “Understanding Static SRAM Operation”
  2. John F Wakerly, “Digital Design Principles and Practices”.
  3. Christiensen D.C.Arandilla, Anastacia B Alvarez “Static Noise Margin of 6T SRAM Cell in 90nm CMOS” 2011 UKSim 13th International Conference on Modeling and Simulation

1. TOOLS USED
   * + Schematic Editor - Cadence Design Tool Kit - Schematic Editor
     + Layout Editor - Cadence Design Tool Kit - Virtuoso
     + Design Rule Checker – Mentor Graphics Calibre LVS
     + Layout vs Schematic tool – Mentor Graphics Calibre LVS
     + Parasitic Extraction – Mentor Graphics Calibre PEX

1. **Architecture**
   1. ARRAY PARTITIONING

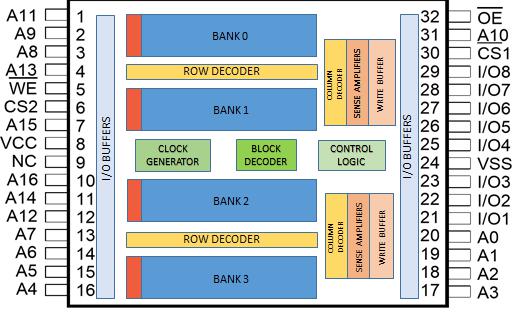
The entire memory is divided into 4 banks each of 256kb. In order to reduce the bit line capacitance, it was decided to have 1024 rows and 256 columns per bank. The motive behind this division is to reduce the power dissipation by keeping all the other memory blocks in retention mode.

1. ADDRESS LINES DISTRIBUTION

• Address lines :- A16 – A0

* + Block Decoder :- A15 – A16
  + Considering temporal and spatial locality, MSB address lines are allocated to block decoder, so that memory blocks need not to be switched frequently.
  + Row Decoder:- A4-A9,A11-A14
  + Column Decoder:- A0-A3,A10

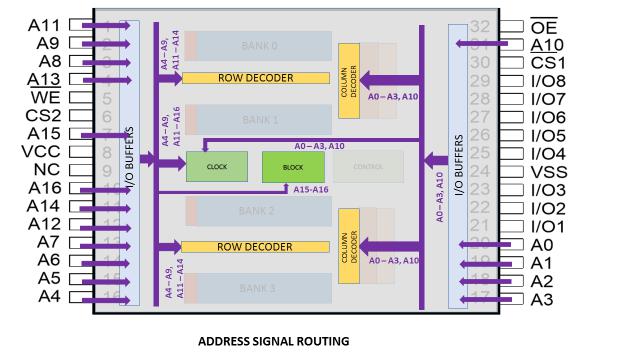
1. FLOOR PLAN



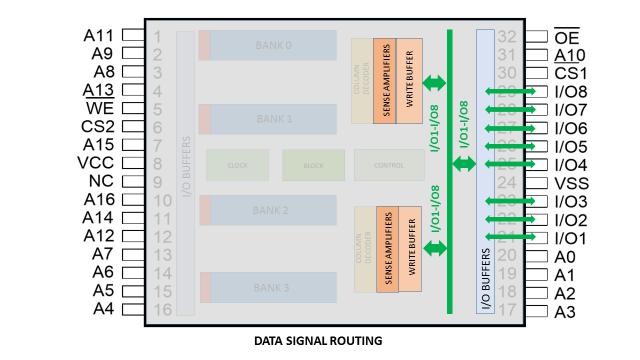
**Figure 2: Floor Plan**

The figure above shows the initial floor plan of the SRAM. Memory is divided in 4 blocks. These blocks are arranged such that row decoder, column decoder, sense amplifier, Write buffer are shared between two memories blocks.

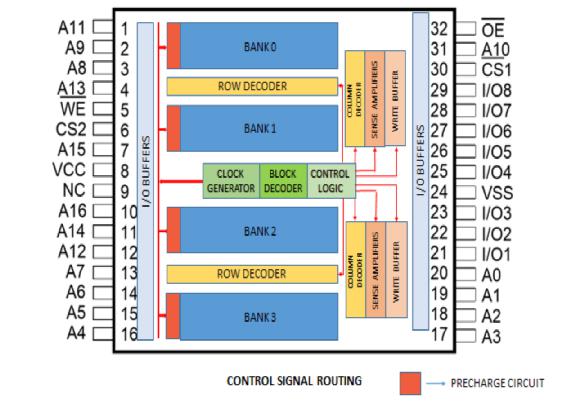
1. ADDRESS SIGNAL ROUTING



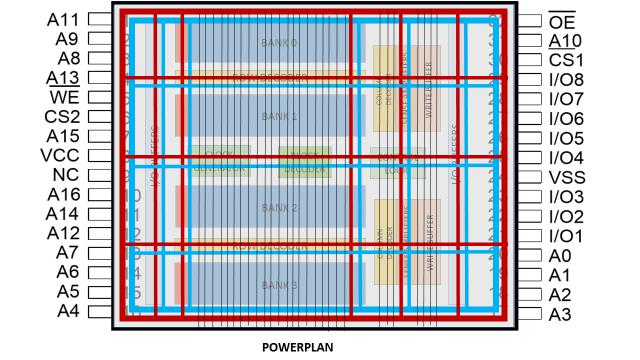
1. DATA SIGNAL ROUTING



1. CONTROL SIGNAL ROUTING



1. POWER PLAN



1. Metal Layer Strategy:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **COLOUR** |  | **METAL LAYER** |  | **CONNECTION** |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 9 |  | VDD |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 8 |  | VSS |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 7 |  | ADDRESS SIGNALS (A0 – |  |
|  |  |  |  |  | A16), WL SIGNALS |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 6 |  | DATA SIGNALS (I/O1 – I/O8) |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 5 |  | CONTROL SIGNALS |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 4 |  | BUSES (ADDR, DATA AND |  |
|  |  |  |  |  | CONTROL) |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 3 |  | Local Routing, BL, BL’ |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 2 |  | Local Routing, GND(local) |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | METAL 1 |  | Local Routing, VDD(local) |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

1. **Detailed Design**
   1. CELL AND CORE DESIGN
2. Cell Type

Static 6-T cell is chosen for SRAM cell design. This topology has the following advantages over 8T and 9T SRAM cell.

* Less static power dissipation
* Occupies less area
* Less read and write delays

Moreover, 4T SRAM cells have poor stability as compared to 6T SRAM cells

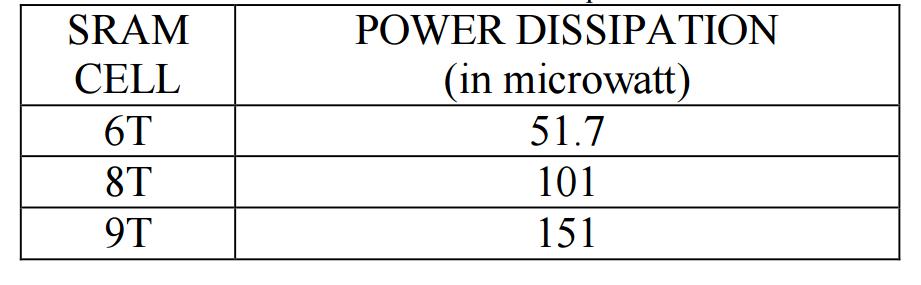


Table 1: Power Dissipation in different SRAM Topologies

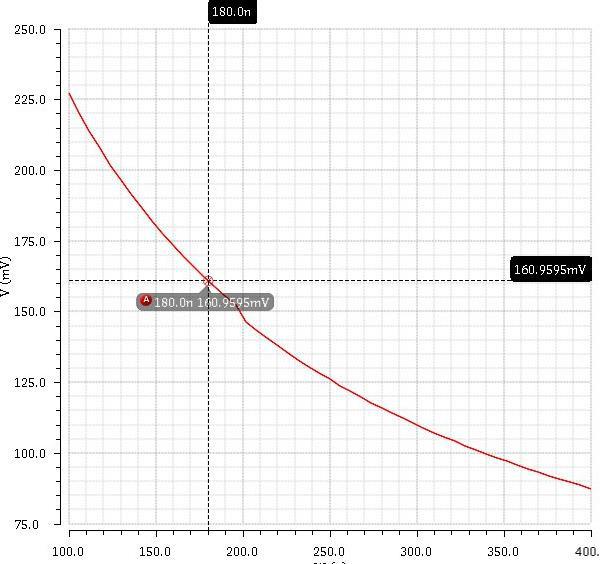
**AREA ESTIMATION**

Typical 6T SRAM Cell in 90 nm Technology = 4 um square

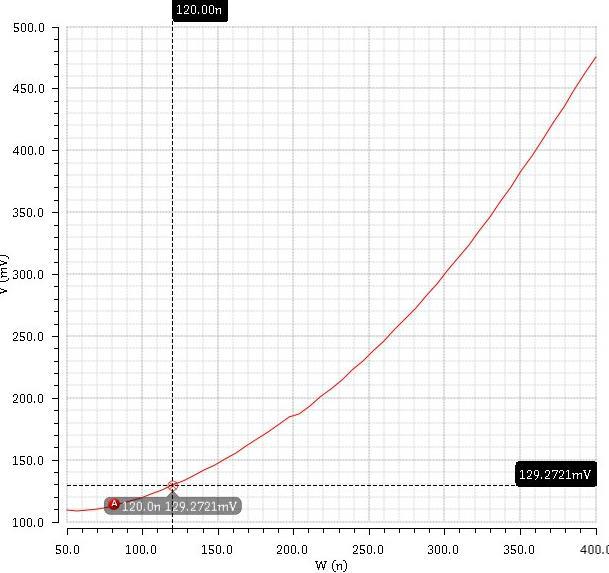
Total number of cells in one bank = 210 x 28 = 262,144

Total Area per Bank = 262,144 X 4 = 1 mm square

Total Memory core Area = 4 mm square



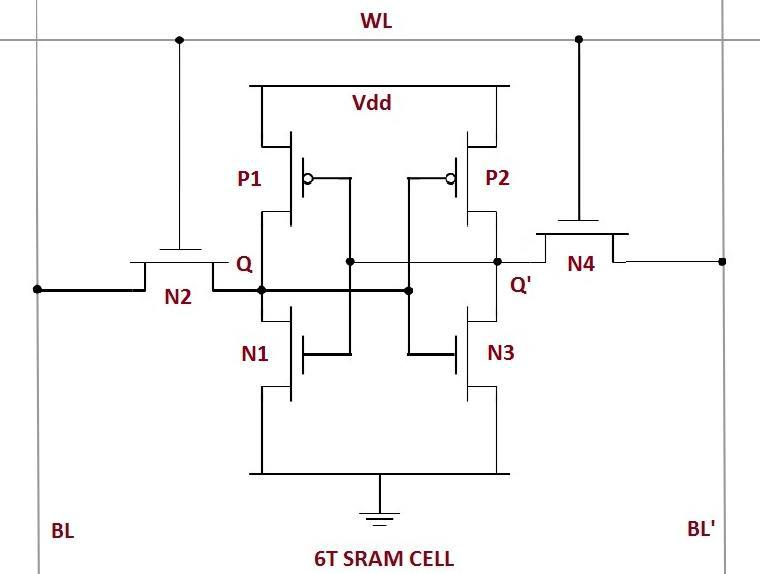
**Figure 4: CR Simulation**



**Figure 5: PR Simulation**

1. Cell Schematic

Simulations were carried out in Cadence Virtuoso to find the bounds on pull -up ratio and cell ratio. Pull-up ratio and cell ratio can be of any value as we are using the high VT transistors, the voltage rise in the internal node will not flip the contents of the cell . Considering acceptable noise margins pull-up ratio was chosen to be 1 and cell ratio was 1.5. Accordingly sizes chosen were as shown in fig. The access transistors were chosen to be of minimum size so as to minimize the bitline capacitance.

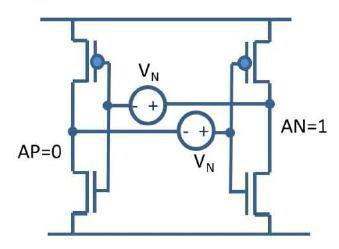


|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Transistor** |  |  | **W/L of Transistor** |  |  |
|  |  |  |  |  |
|  |  |  |  |  |  |  |
|  | **N1,N3** |  |  | (180nm/80nm) |  |  |
|  | **N2,N4** | |  | (120nm/80nm) | |  |
|  |  | |  |  | |  |
|  | **P1,P2** |  |  | (120nm/80nm) |  |  |
|  |  |  |  |  |  |  |

**Figure 6: 6T SRAM Cell Schematic**

4.1.3. Cell Schematic Simulations

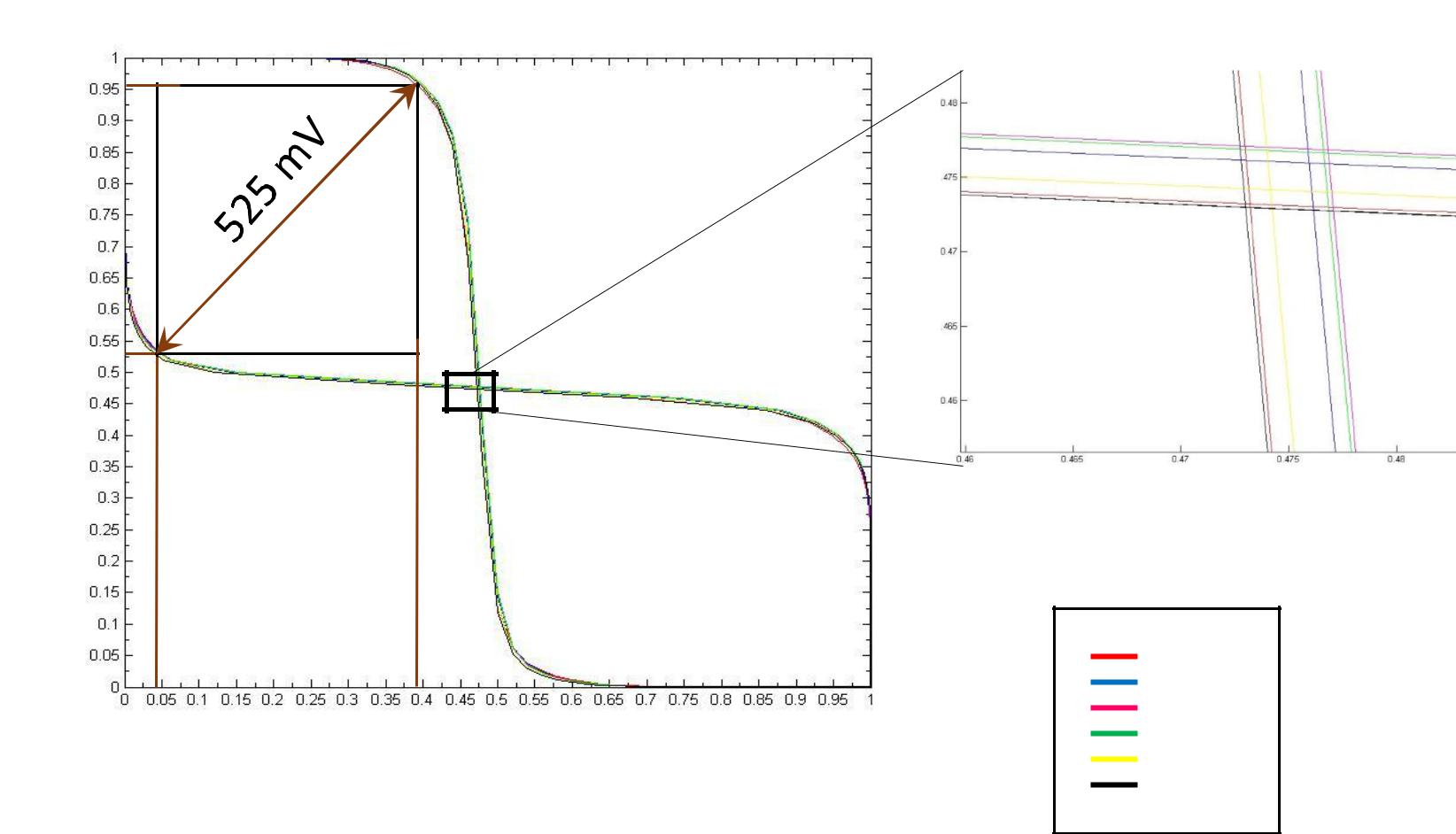
*4.1.3.1. Static Noise Margin:*



**Figure 7: SNM Noise voltage source**

Static noise margin is the maximum noise voltage VN that can occur simultaneously on both the voltage sources as shown in the figure above and will not be able to flip the contents of the cell. The cell is in hold mode during this time. Inverter characteristic is obtained, flipped and maximum Square is determined as shown below

* Static Noise Margin = 525mV



CR = 1

CR = 1.2

CR = 1.4

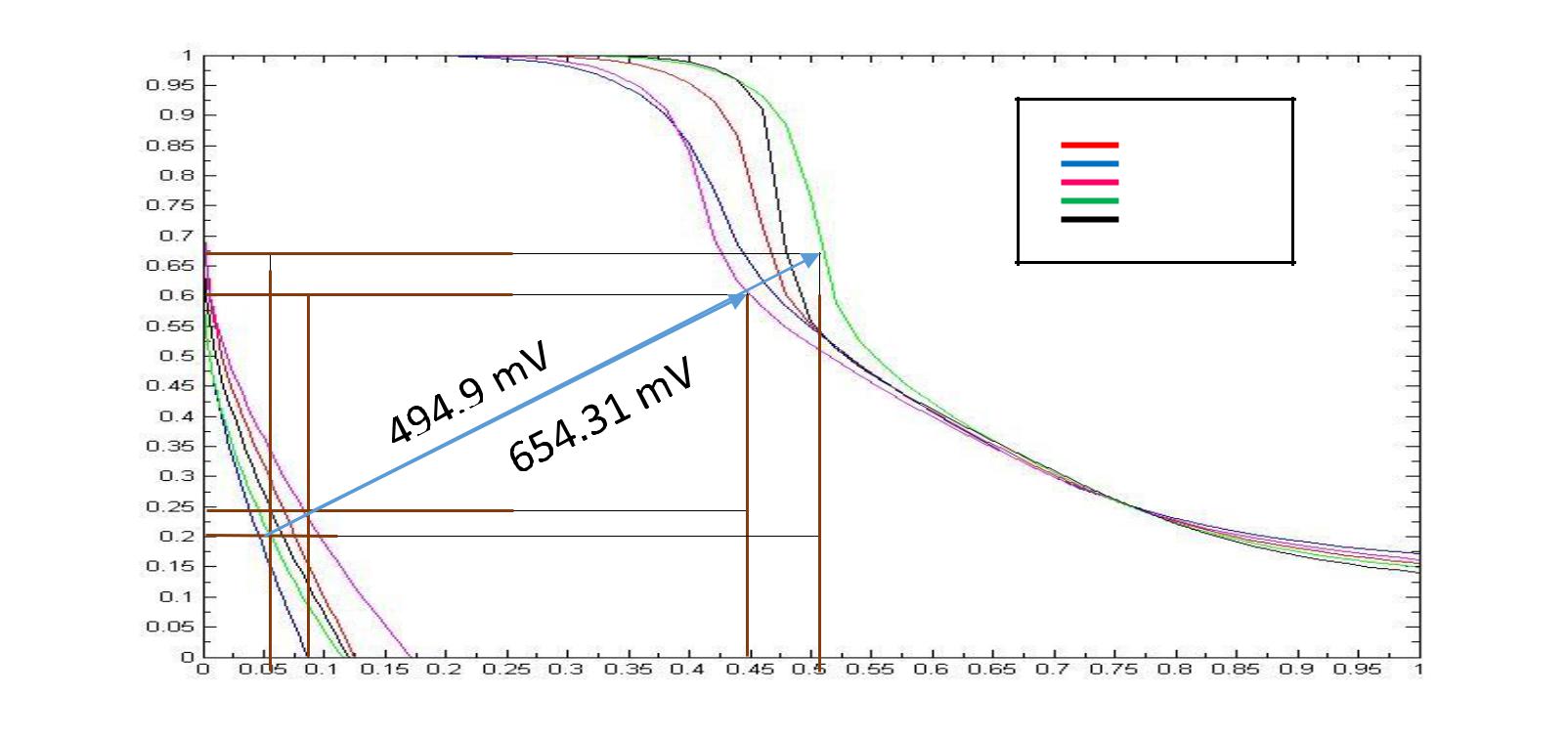
CR = 1.6

**Figure 8: Hold SNM for Different CR Simulation**

*4.1.3.2.* *Write Noise Margin*

Write noise margin is the maximum noise voltage VN that can occur simultaneously on both the voltage sources as shown in above section that will prevent write operation to flip the content of the cell. Cell is put in write mode with word lines enabled and one of the bit lines pulled to ground. The write noise margin for different PVT corners is shown below:

* Worst Write Noise Margin = 654.31 mV



ff fnsp

Average WSNM

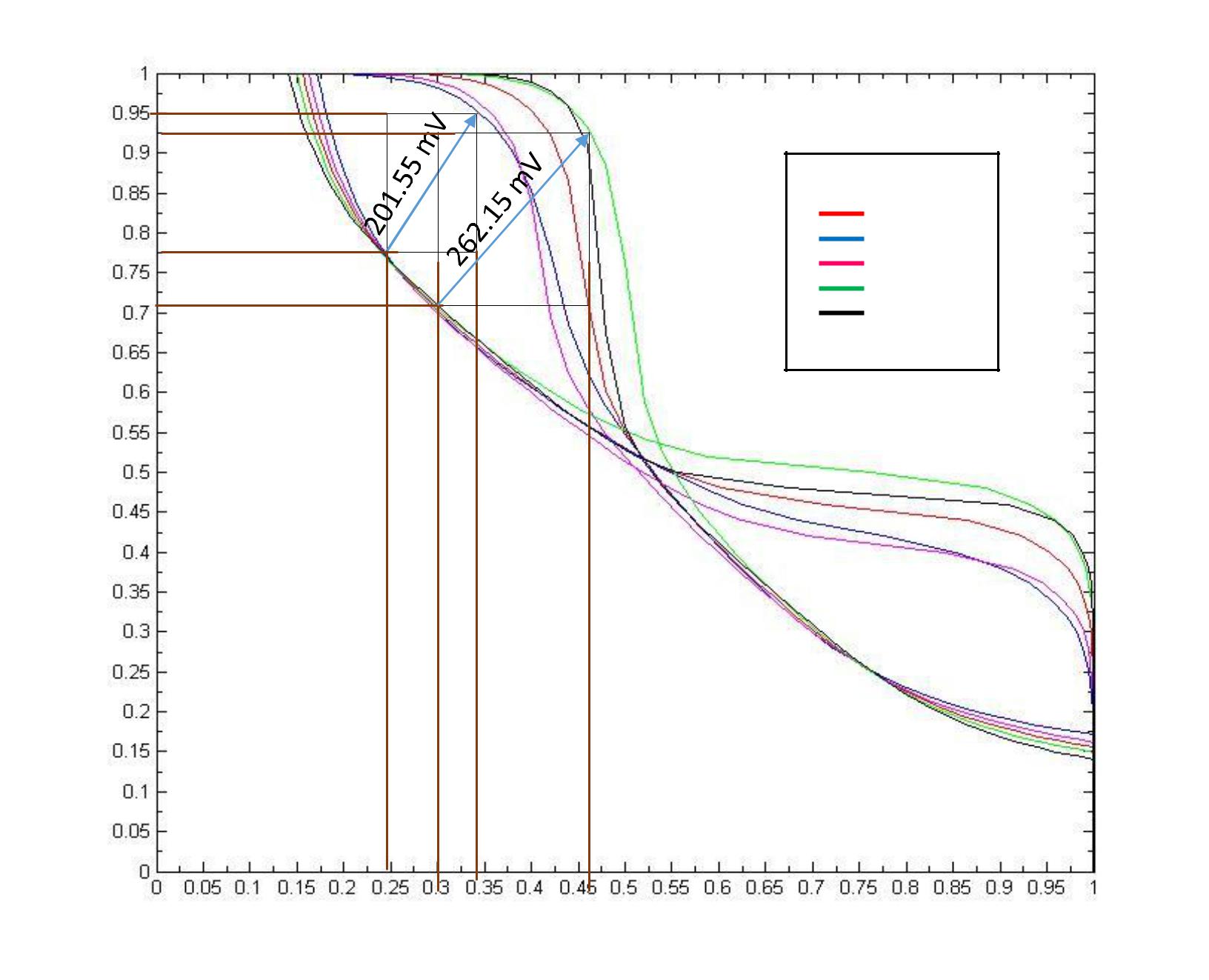
= 622.655 mV

**Figure 9: Write Margin in different PVT corners**

*4.1.3.3.* *Read Noise Margin*

Read noise margin is the maximum noise voltage VN that can occur simultaneously on both the voltage sources as shown in figure 7 that will flip the content of the cell during a read operation. Cell is put in read mode with word line enabled and bit lines tied to VDD. The worst case read noise margin is shown below.

* Worst Read Noise Margin = 262.15 mV



ff fnsp snfp ss

Average RSNM = 231.85 mV

**Figure10: Read SNM for Different Process Corner**

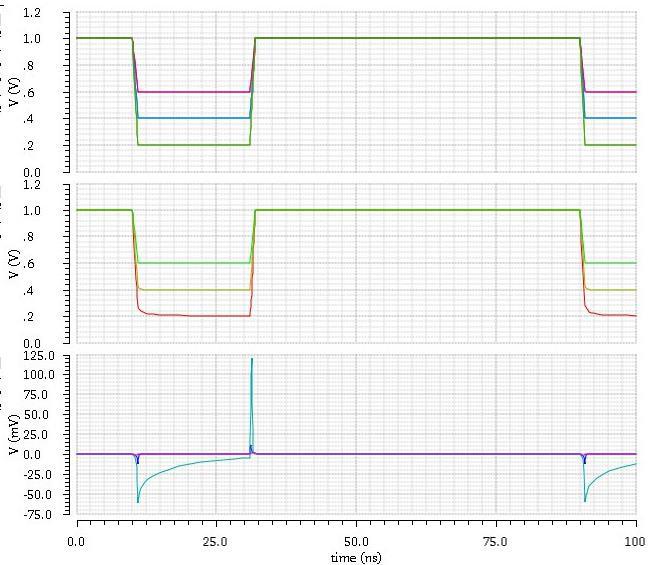
1. Retention Voltage Calculation:

Data Retention Voltage (DRV) is the voltage at which the SNM of the SRAM cell reaches on bringing down VDD.

DRV > Threshold Voltage

From simulation shown below,

DRV lies between 400 and 600 mV.



VDD

Q

Q`

**Figure 9: Retention Voltage Simulation**

Q’ spikes vary with different stepped down VDDs.

4.1.5. Read Current & Write Current For Single SRAM

To calculate read current, simulated single SRAM cell using ideal voltage source of 1V. By setting the initial condition stored 1 in the cell. As 1 is stored in the cell, pull down transistor will discharge the BL\_BAR. Cycle time is used as 85ns, same as data sheet. To calculate the read current considered peak current supplied by the voltage source.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  | Table 1: Read Current measurements | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | ***Temperature*** |  |  |  | ***ff*** |  |  |  | ***ss*** |  |  |  | ***snfp*** |  |  |  | ***fnsp*** |  |  |  | ***tt*** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  | |  |  |  | |  |  |  | | |  |  |  |  |  |  | |  |  |  | | |  |  |
|  |  | *-40* |  |  |  | *56.83* |  |  |  | *27.51* |  |  |  | *33.73* |  |  |  | *49.04* |  |  |  | *41.38* |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | |  |  |  | |  |  |  | | |  |  |  |  |  |  | |  |  |  | | |  |  |
|  |  | *27* |  |  |  | *52.86* |  |  |  | *25.69* |  |  |  | *31.45* |  |  |  | *45.63* |  |  |  | *38.42* |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  | |  |  |  | |  |  |  | | |  |  |  |  |  |  | |  |  |  | | |  |  |
|  |  | *85* |  |  |  | *49.11* |  |  |  | *24.29* |  |  |  | *29.6* |  |  |  | *42.38* |  |  |  | *35.92* |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

*Note:- Currents are in uA*

1. Write Current for Single SRAM in Active mode:

To calculate write current, simulated single SRAM cell using ideal voltage source of 1V. By setting the initial condition stored 1 in the cell. Flipped the content of cell, to zero. Cycle time is used as 85ns, same as data sheet. To calculate the write current, considered peak current supplied by the voltage source.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | Table 2: Write Current measurements | | | | |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ***Temperature*** |  | ***ff*** |  | ***ss*** |  |  | ***snfp*** |  |  | ***fnsp*** |  | ***tt*** |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | |  | |  |  |  |  |  | |  | |  |  |
|  |  |  |  |  |  |  | *59.85* |  |  |  |  |  |  |  |
| *-40* |  | *93.56* |  | *49.68* |  |  |  |  | *82.28* |  | *71.2* |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| *27* |  | *90.12* |  | *47.87* |  |  | *57.56* |  |  | *79.22* |  | *68.38* |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| *85* |  | *85.82* |  | *45.76* |  |  | *54.92* |  |  | *75.29* |  | *65.07* |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

*Note:- Currents are in uA*

4.1.7. Leakage Current in Active and Retention Mode:

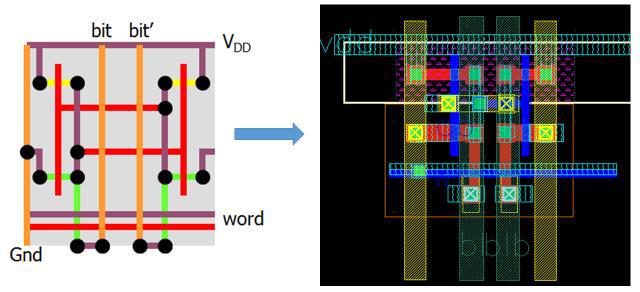
Leakage current are calculated for single SRAM cell in hold mode for 1V (active mode).

Table 3: Leakage Current measurements

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Temperature** |  |  |  | **ff** |  |  |  | **ss** |  |  |  | **snfp** |  |  |  | **fnsp** |  |  |  | **tt** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  | | |  |  | | |  |  | | |  |  | | |  |  | | |  |  |  |
|  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  |
|  | -40 |  |  |  | 0.645 |  |  |  | 0.098 |  |  |  | 0.24 |  |  |  | 0.261 |  |  |  | 0.249 |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  |
|  | 27 |  |  |  | 1.45 |  |  |  | 0.1 |  |  |  | 0.374 |  |  |  | 0.358 |  |  |  | 0.311 |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  |
|  | 85 |  |  |  | 6.2 |  |  |  | 0.16 |  |  |  | 1.26 |  |  |  | 1.15 |  |  |  | 0.8 |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Currents are in nA

4.2 CELL LAYOUT



**Figure 15: SRAM Cell Layout**

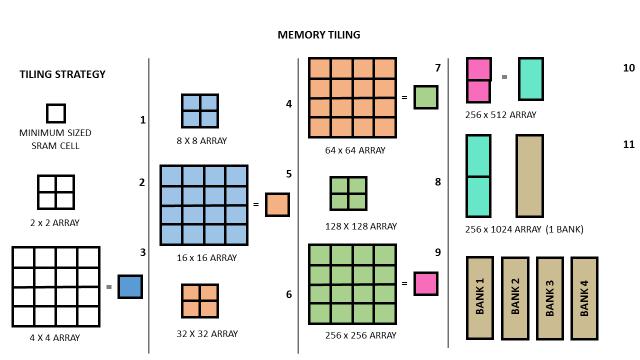
4.2.2 Summary of cell:

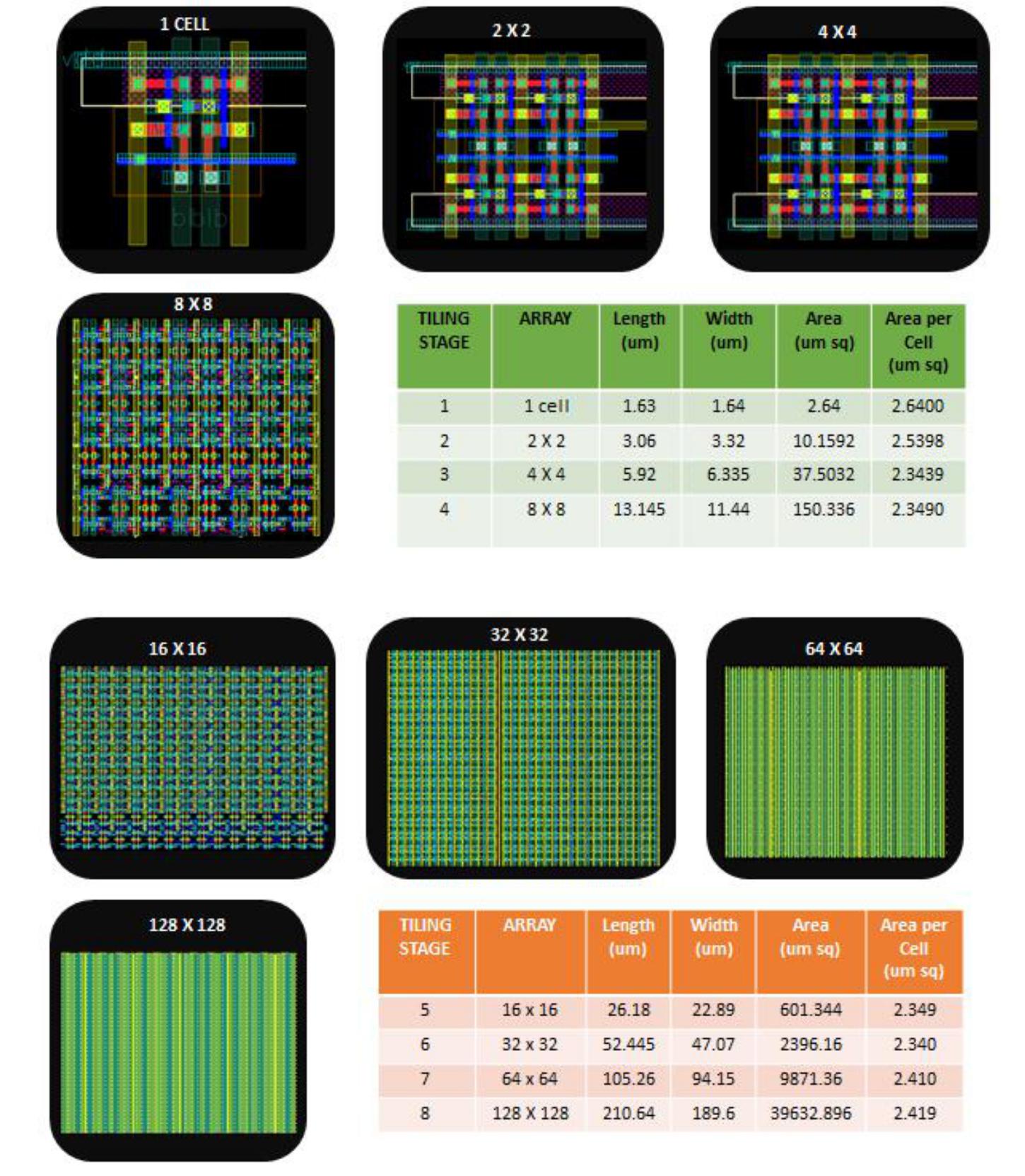
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **Length** |  |  |  | **Width** |  |  |  | **Area** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  | **(um)** |  |  |  | **(um)** |  |  |  | **(um sq)** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | |  |  | | |  |  | | |  |  |  |
|  |  | 1.63 |  |  |  | 1.64 |  |  |  | 2.64 |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Table 4: Summary of Cell

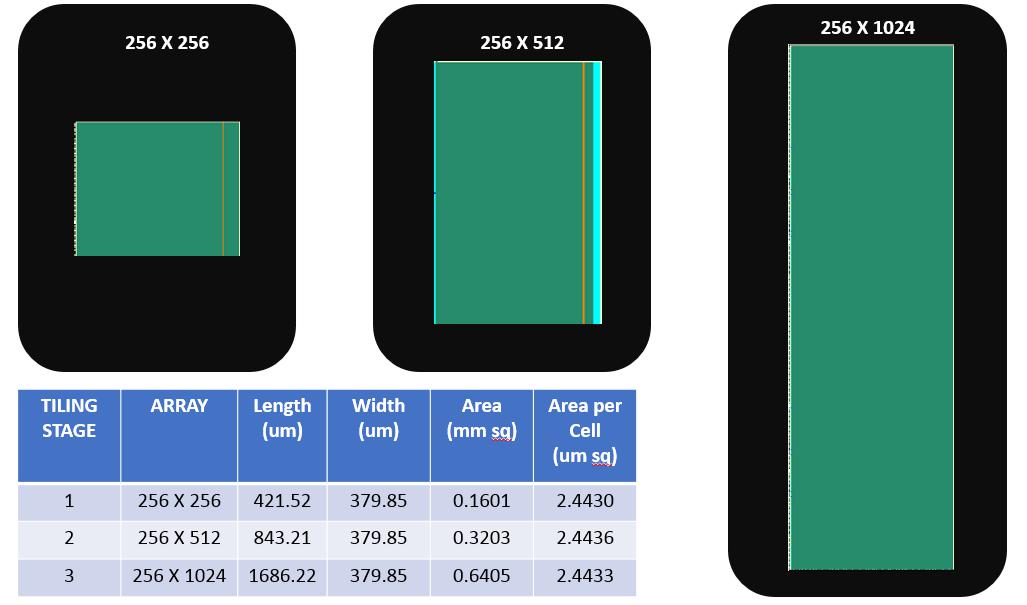
4.3. CORE LAYOUT

4.3.1 Core Assembly:



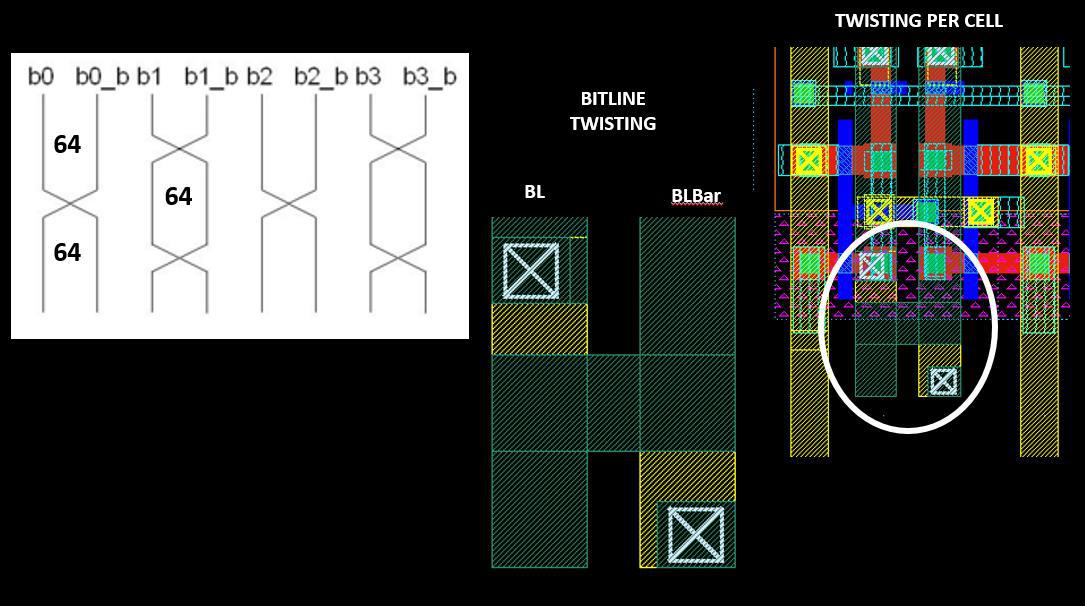


**Figure 12: optimized SRAM 4\*4 cell**

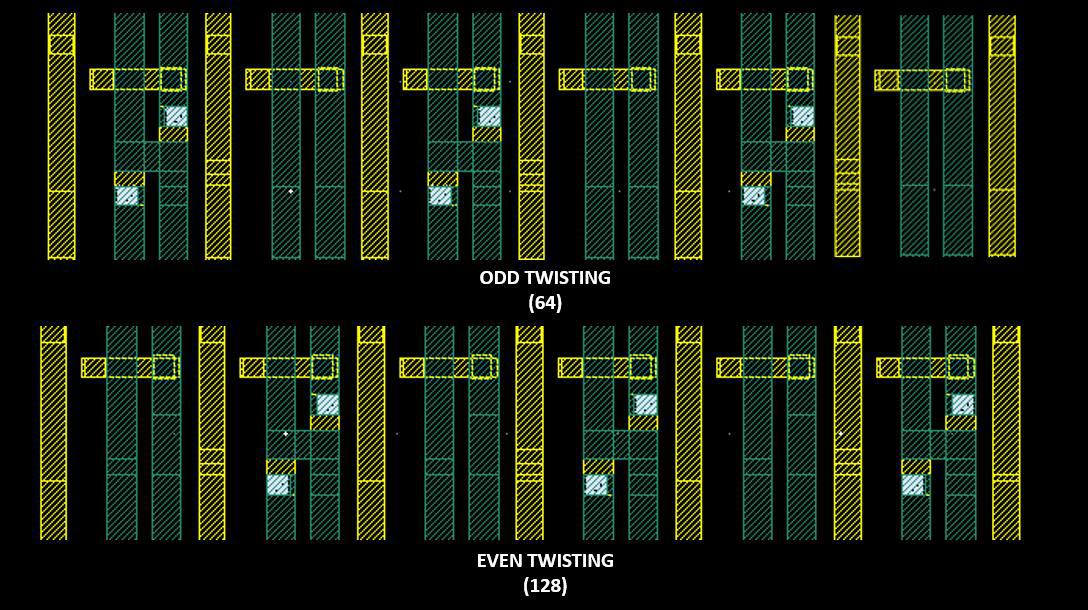


**Figure : Tiling (contd)**

1. Bit Line Twisting



**Figure 18: Bit line Twisting**



**Figure : Odd and Even Twisting Pattern**



**Figure : Mirrored Twists**

1. Core Summary

Table 5: Core Summary

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Parameters** |  | **Values** |  | **Units** |  | **Comments** |
|  |  |  |  |  |  |  |  |
|  | **Height** |  | 1686.22 |  | um |  | 1024 rows |
| **Length** | | 379.85 | |  | um |  | 256 columns with substrate connections |
|  | |  | |  |  |  |  |
|  | **Area** |  | 0.6405 |  | (mm)2 |  | For 1 Bank |
|  |  |  |  |  |  |  |  |
|  | **Retention Voltage** |  | 500 |  | mV |  | Typical |
| **Read cycle power** | | 10.64 | |  | uW |  | 200ff BL cap |
|  | |  | |  |  |  |  |
|  | **Leakage current** |  | 140 |  | nA |  |  |
|  | **BL Read propagation Delay** |  | 900 |  | ps |  | BL to reach 80mV (with 1024 cells) |
| **BL Write propagation Delay** | | 535 | |  | ps |  | BL to reach the cell (with 1024 cells) |
|  | |  | |  |  |  |  |
|  | **Min Write pulse width** |  | 2 |  | ns |  | Time to flip cell content |
| **WL propagation delay** | | 305 | |  | ps |  | WL prop delay (with 256 cells) |
|  | |  | |  |  |  |  |
|  | **Cap of BL, BLB** |  | 586 |  | fF |  | Cc Extracted for 1024 rows |
| **Cal of WL** | | 686 | |  | fF |  | Cc Extracted for 512 columns |
|  |  |  |  |  |  |  |  |

1. DECODING SCHEME

Hierarchical scheme has been used for the design of row decoders. The decoder block is divided into 2 Stages:

* + The Row Decoder is split into two 5 to 32 pre-decoders and an array of 1024 AND gates, used to generate Word Line Enable signals.
  + Between successive Read/Write cycles, the word line must be pulled to ground to avoid crosstalk of various SRAM cells and/or to pre-charge the bit lines.
  + This cycle is synchronized by the ATD block which generates an active high pulse to enable the array of AND gates.
  + The Row Decoder worst case delay was observed keeping the ATD\_EN high and switching the row address from 0000000000 to 1111111111.
  + To get an estimate of power consumption, we decoded 32 contiguous addresses, switching the pre-decoder from 0 to 31. This provides us with a fairly accurate estimate of average power consumption in the circuit.

1. **Optimized Pass transistor based NAND gate:**

To solve the above problem we decided to optimize the pass transistor logic. In this architecture we implemented two input NAND function with two transistors one n-FET and one p-FET so that area is very much reduced. NAND functionality is obtained by connecting one of the input to the gate terminal directly while inverted of the other input to the source terminal. One of the special attributes of this circuit is that it can be at least as fast as an inverter if the branching effort of the source input is sufficiently large and if the total capacitance on the source line is much greater than the output load capacitance for the gate.

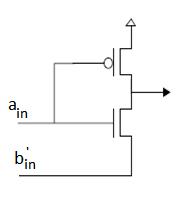


Figure Optimized pass transistor based NAND gate

Table Truth table of Optimized pass transistor based NAND gate

|  |  |  |  |
| --- | --- | --- | --- |
| **Ain** | **Bin** | **Bin’** | **output** |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

Table Gate capacitances Comparison for different architectures

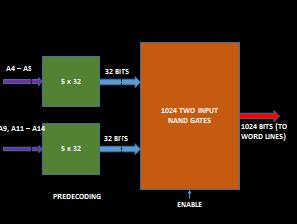
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Capacitance** |  |  | **Value** | |  |  |
|  | CMOS inverter |  |  | 9.25884 fF | |  |  |
|  | 2 input conventional NAND gate | |  | 17.8557 fF | |  |  |
|  | 4 input NOR style NAND gate | |  | 18.66474 fF | | |  |
|  | Optimized pass transistor based NAND gate | |  | 13.89 fF | |  |  |
|  | Table Power delay comparison of different architectures | | | | |  |  |
|  | **Architecture** | **Power Dissipation** | | **Delay(ps)** |  | **Delay-Power Product** | |
|  |  | **(μW)** | |  |  | **(μW- ps)** | |
|  | Conventional NAND Gate | 19.67 | | 2623 |  | 51594.41 |  |
|  | Nakamura’s NAND Gate | 11.32 | | 512 |  | 5795.84 |  |
|  | NOR Style NAND Gate | 1.26 | | 96 |  | 120.96 |  |
| Optimized pass transistor based NAND Gate | | 0.72 | | 90 |  | 64.8 |  |

1. Simulation Results:

Table 6: Decoder Power Calculations

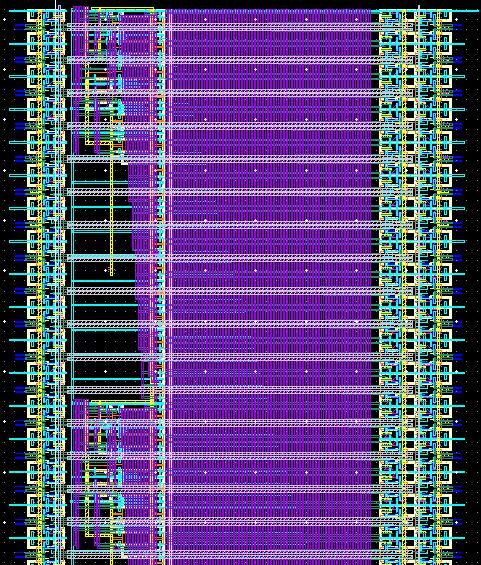
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Worst Case** |  | **Peak Current(mA)** |  | **RMS** |  |  | **Average** |
|  | **Delay(ps)** |  |  |  | **Current(uA)** |  |  | **Current(uA)** |
|  |  |  |  |  |  |  |  |  |
|  | 303 |  | 4.12 |  | 88 |  |  | 32.16 |
|  |  |  |  |  |  |  |  |  |

1. Block Diagram of Row Decoder:



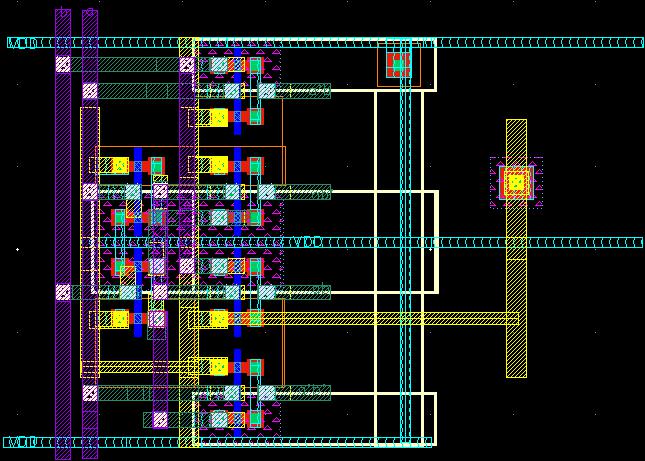
**Figure 19: Block Diagram of Row Decoder**

1. DECODER Circuit Layout:

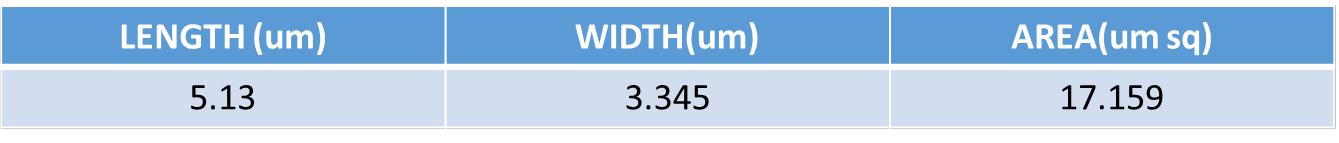


**Figure 20: Layout of Row Decoder**

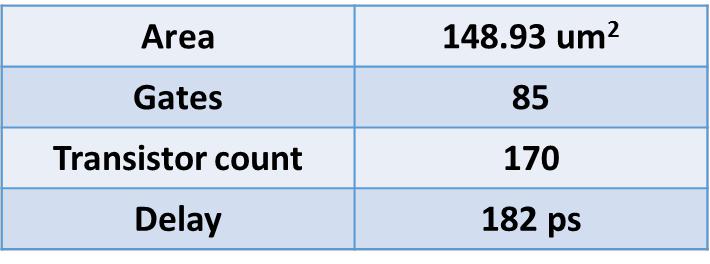
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **L (um)** |  |  |  | **W(um)** |  |  |  | **Area (um** |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  | **sq)** |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | |  | | | |  |  |  |  |  |  |
|  |  | |  |  |  | |  |  |  | 72265.34 |  |  |
|  |  | 42.83 |  |  |  | 1687.26 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | **Table 7:Row Decoder Specs** | | | | | | |  |  |  |



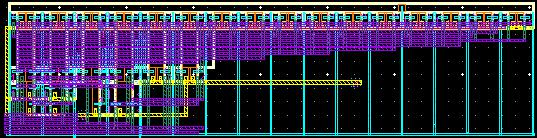
**Figure 21: Layout of Block Decoder**



**Table 8:Block Decoder Specifications**

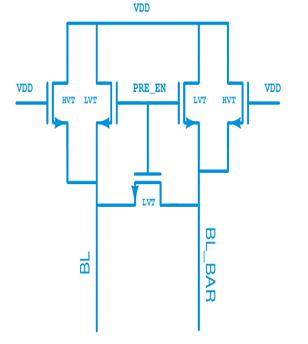


**Table 9: Column Decoder Specifications**

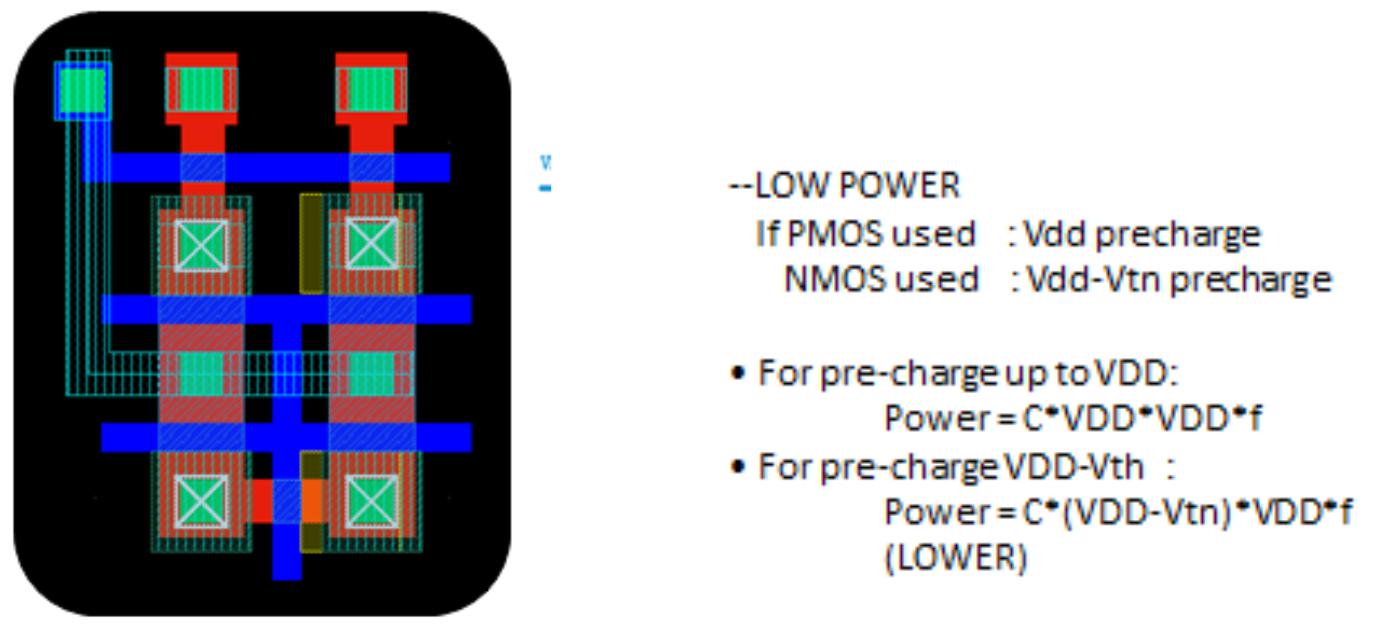


**Figure 22: Layout of Column Decoder**

1. CORE I/O:
2. Pre charge Circuitry:



1. Pre charge circuit layout



**Figure 26:- Precharge circuit layout**

4.5.2. Sense amplifier

Traditionally a large number of SRAM bit cells, 1024 in this case, are connected to a common bit-line to get the highest density and array efficiency. This results in a large capacitance on the bit lines. Hence any differential voltage on these bit lines would take a long time to split to full CMOS levels. Hence we require additional circuitry called “SENSE AMPLIFIER” which detect small differential voltages on the two bit lines and process it to yield full CMOS voltages. Sense amplifiers are categorized into broad 3 categories:

* VOLTAGE MODE SENSE AMPLIFIER: Sense amplifiers which detects the voltage difference on the bit lines are called voltage mode sense amplifiers.
* CURRENT MODE SENSE AMPLIFIERS: Sense amplifier which detects the current difference in the bit lines are called Current mode sense amplifiers.
* CHARGE TRANSFER SENSE AMPLIFIERS: The Charge Transfer Sense Amplifier (CTSA) operates by making use of the charge redistribution from high capacitance bit-lines to the low capacitance sense amplifier output nodes [4]. This results in high speed operation and lower power consumption due to low voltage swing on the bit-lines

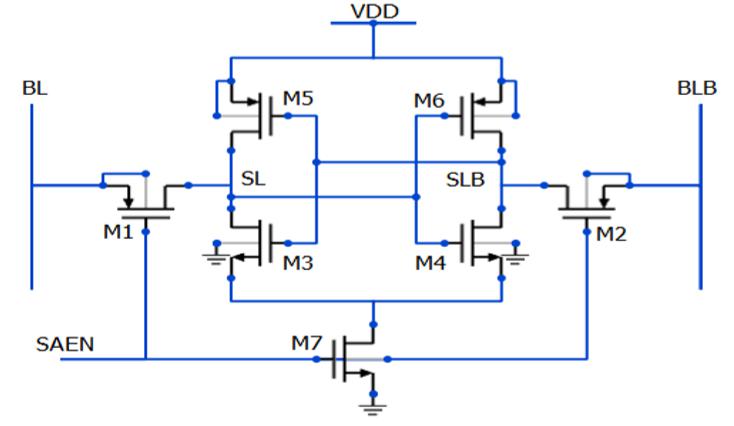
Of all the three above mentioned topologies available, we chose to implement Voltage Mode Sense Amplifier.

A paper published in International Journal of Emerging Trends & Technology in Computer Science (IJETTCS) titled

“Performance of Various Sense Amplifier Topologies in sub100nm Planar MOSFET Technology” by Parita Patel,

Sameena Zafar and Hemant Soni lists a number of topologies available for a sense amplifier of which we considered one of them.

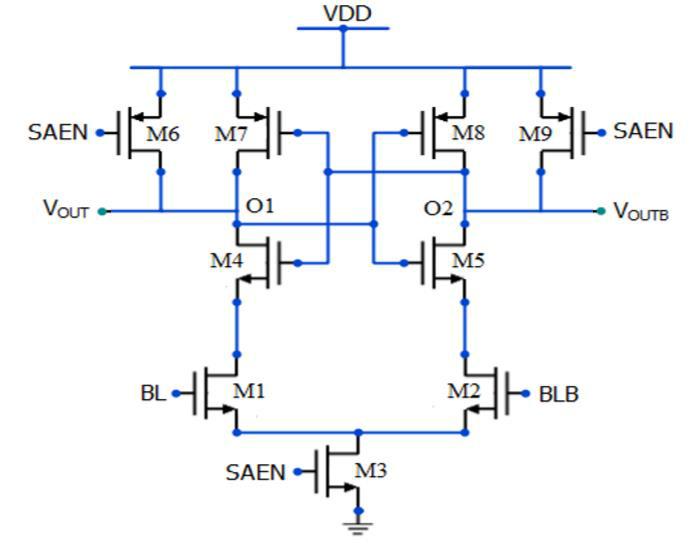
**Topology 1**:Cross Coupled Voltage Mode SA:



*Fig : Cross Coupled Voltage Mode SA*

WORKING: In the Cross-coupled voltage mode SA, M1 and M2 are the access transistors, whereas M3 M6 forms cross-coupled inverters. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. Due to positive feedback, higher voltage level goes to VDD and the other level goes to ground. The nodes SL and SLB are input and output terminals at the same time. Therefore, the circuit cannot be connected directly to the bit line since the circuit would attempt to discharge the bit line capacitance during the decision phase and would increase delay and power. A solution is to separate the bit lines and the output of the sense amplifier. This way the voltage swing at the bit lines can easily reduce by half, resulting in lower speed and noise margin. Hence we went ahead with the second Topology: Current latched voltage mode SA.

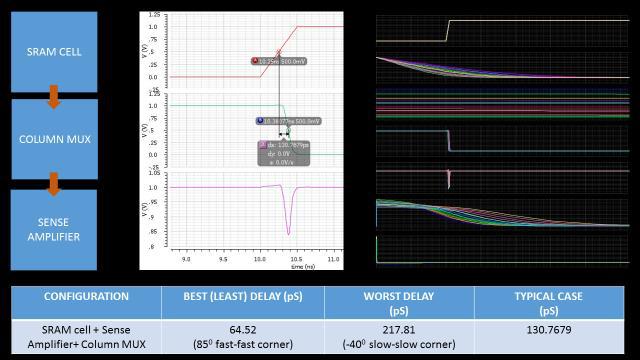
**Topology 2**:Current latched voltage mode SA



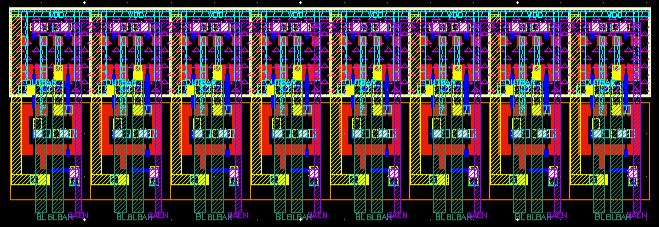
*Fig : Current latched voltage mode SA*

WORKING: This sense amplifier combines strong positive feedback with a high resistive input. The current flow of the differential input transistors M1 and M2 controls the serially connected latch circuit. A small difference between the currents through M1 and M2 converts to a large output voltage. This current latched SA is faster than conventional cross coupled SA. During reset phase when SAEN=0V, the output nodes of the SA (O1 and O2) are reset to VDD through the reset transistors M6 and M9. During evaluation phase when SAEN=VDD, M3 turns ON and the input transistors M1 and M2 starts to discharge O1and O2 node voltages to GND. When any of these node voltages falls from VDD to VDD-Vthn, NMOS transistors of the cross coupled inverters turn ON initiating positive feedback. Further when any of output node voltage drops to VDD-Vthp, PMOS transistors of the inverters turns ON and further enhances the positive feedback and converts a small input voltage difference to large full scale output. Here the bit lines and output are independent of each other. Hence the advantage.

1. *Simulation Results*



1. *Layout*



**Figure 29: Layout of Sense Amplifier**

2

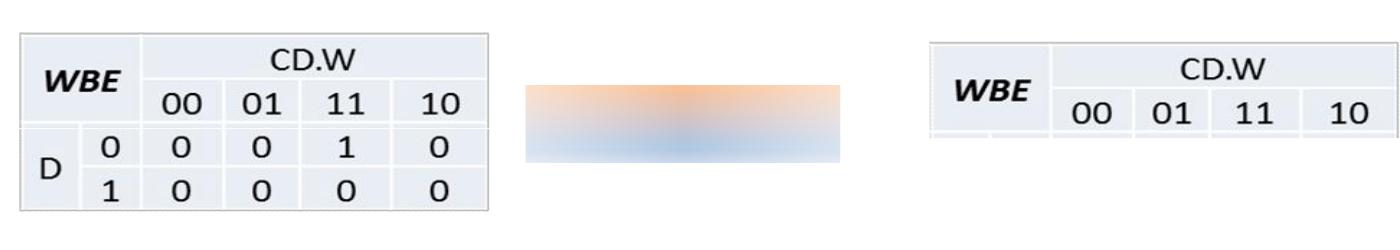
Sense Amplifier (width = 9.5um height = 1.9um Area = 18.05um )

1. Write Buffer

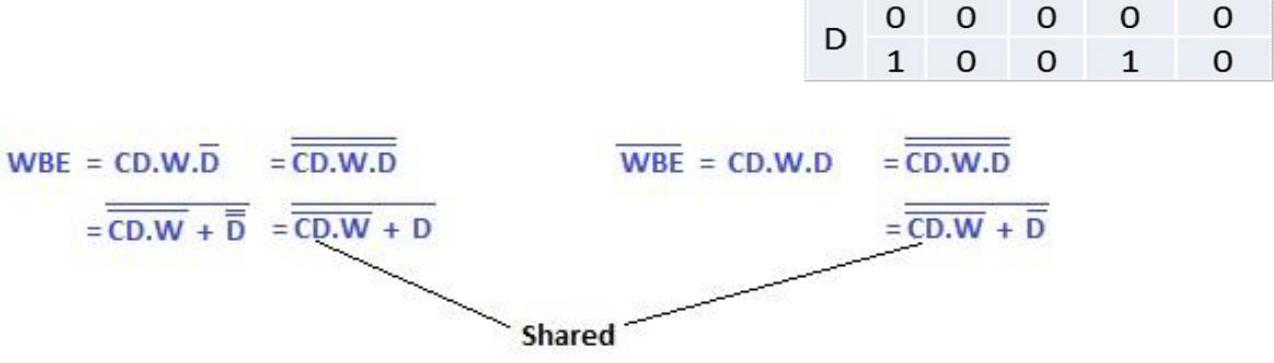
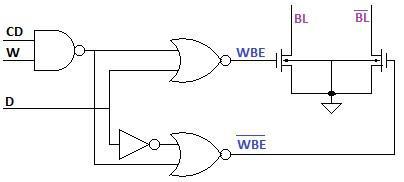
Write buffer discharges the bit-line or the complement as required by the input data to be written to the cell.

*4.5.3.1.* *Logic Design and Circuit Schematic*

The K-maps and the logic derivation is shown below.



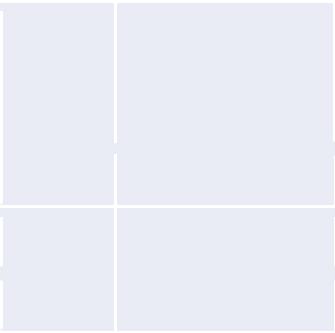
**Logic Design**



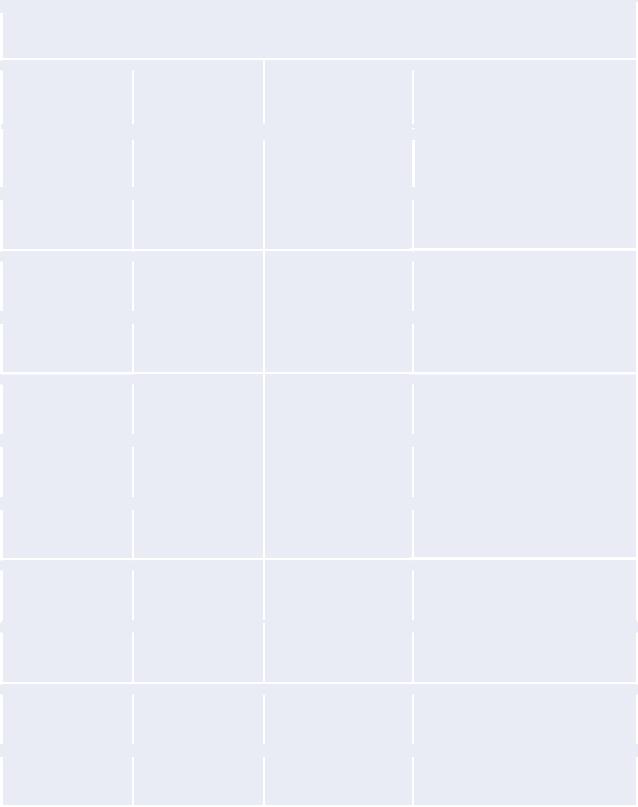
**Figure 30: Schematic of Write Buffer**

1. *Simulation Results*

Table11: Write Buffer Discharge Time and Delay Calculation

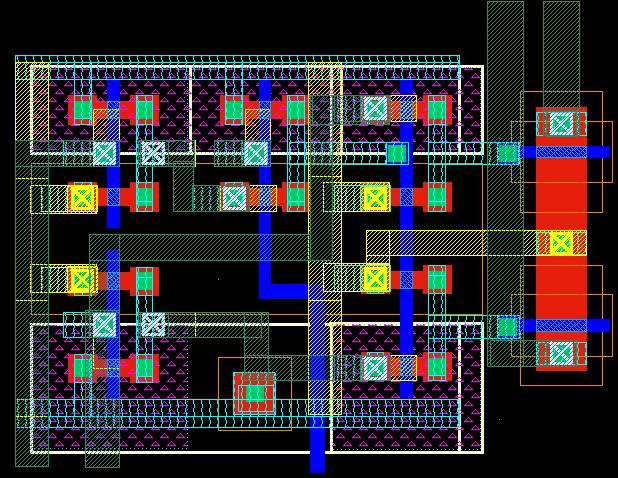


|  |  |
| --- | --- |
|  | **Discharge** |
|  | **(90%) Time** |
| **Cap (fF) (ns)** | |
| 300 | 0.928 |
| 400 | 1.18 |
| 500 | 1.48 |

***Load = 400fF; Driver: 1um/80nm)***

|  |  |  |  |
| --- | --- | --- | --- |
| **P** | **V (v)** | **T (C)** | **Delay (ns)** |
| TT | 1 | 27 | 1.18 |
| SS | 1 | 27 | 1.58 |
| FF | 1 | 27 | 0.96 |
| SS | 1 | -25 | 1.53 |
| SS | 1 | 125 | 1.72 |
| FF | 1 | -25 | 0.92 |
| FF | 1 | 125 | 1.03 |
| SS | 0.9 | 125 | ***1.99*** |
| SS | 1.1 | 125 | 1.51 |
| FF | 0.9 | -25 | 1.05 |
| FF | 1.1 | -25 | ***0.84*** |

*4.5.3.3.* *Layout*



**Figure 31: Layout of Write Buffer**

2

Write Buffer (width = 9.6um height = 1.7um Area = 16.32um )

1. ATD scheme

The ATD (Address Transition Detection) circuit is heart of the Asynchronous SRAM memory chip. It decides total operation of the memory chip. Unlike the synchronous SRAM design which suffers from clock skew, synchronization with external inputs etc where as an Asynchronous SRAM design responds to any address transition in the signal. This operation is very fast but it also suffers from problems which lead to undesired operation due to change in the address signal because of noise.

To overcome this problems ATD circuit was used, which will check for address transition and generates a stretched pulse for the internal circuit to perform its operation. Until the pulse generated we can keep the rest of the circuit of memory chip can be in non-operating mode. The ATD scheme was implemented by two stages. First stage is pulse generator circuit and other is pulse stretching circuit.

4.6.1. ATD inputs

Table 12 ATD Inputs

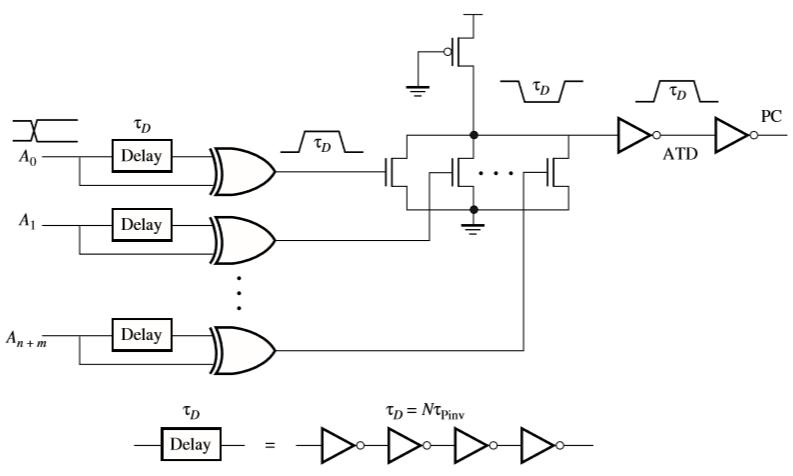
|  |  |  |
| --- | --- | --- |
| **S.No** | **Inputs** | **Sources** |
| 1 | A0-A18 | Input buffers |
| 2 | CE | Input buffers |

4.6.2. ATD outputs

Table 13 ATD Outputs

|  |  |  |
| --- | --- | --- |
| **S.No** | **Outputs** | **Sinks** |
| 1 | ATD\_OUT | Tile level Control Circuit |

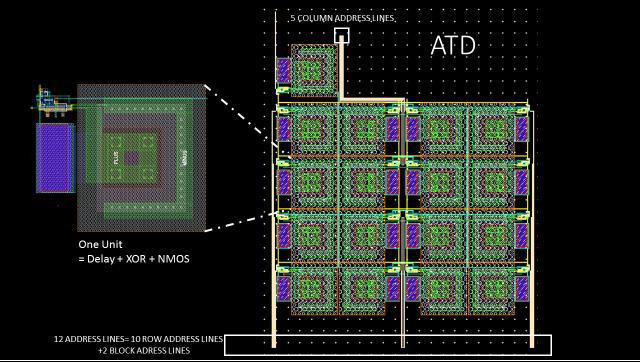
4.6.3. ATD Circuit:



**Figure 32: ATD Pulse generator Circuit Schematic**

The ATD pulse generator circuit detects the transition in any one of 19 address signals and generates the pulse of 200ps width. The ATD pulse generator incorporated delay circuit of 200ps in all of the address chain. The 200ps delay circuit was implemented using simple inverter chain.

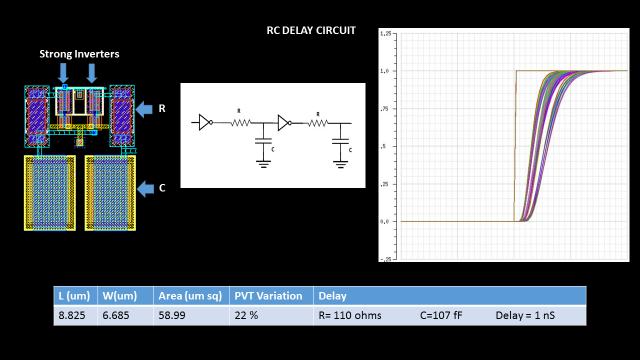
**ATD LAYOUT**

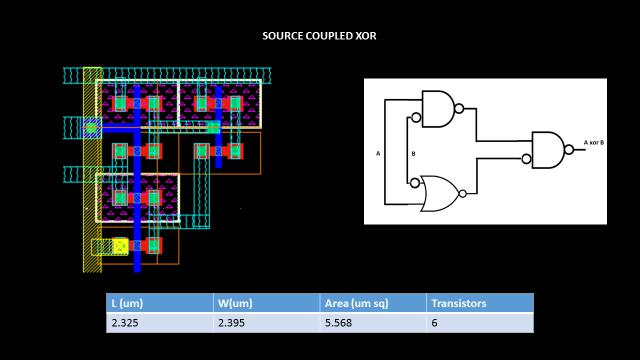


W=109.82 um

L=127.47 um

Area= 13998.7 um square

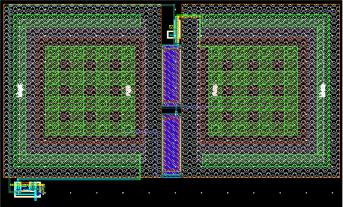




**Figure 33: Layout of Delay (200ps) circuit**

4.6.5. ATD Pulse Stretching Circuit:

The pulse width of ATD pulse generated by pulse generator is not sufficient for ASRAM to perform its operation. This pulse needs to stretch and can be used for generating necessary control signals. The pulse stretching circuit consists of SR latch and large delay circuit (5ns).



**Figure 34: ATD pulse stretching circuit**

4.6.6. Delay Circuit (5ns):

The operation of memory chip depends upon the ATD pulse. The ATD pulse in turn depends upon operation of delay circuit. Hence this delay circuit operation is critical in our design. The delay circuit operation should be PVT invariant to generate proper ATD pulse width.

No of circuits are implemented and operation of each of it evaluated. The following lists some of approaches used in this implementation.

1. Inverter Based Approach
   1. Approach –I (Capacitance variation)
   2. Approach –II (Resistance variation)
2. Variable Delay using Thyristor Based Approach
3. RC based Delay with Strong inverters



Layout of Delay (5 ns)

1. Group Level Control circuit:
2. GLC inputs

Table 14. GLC Inputs

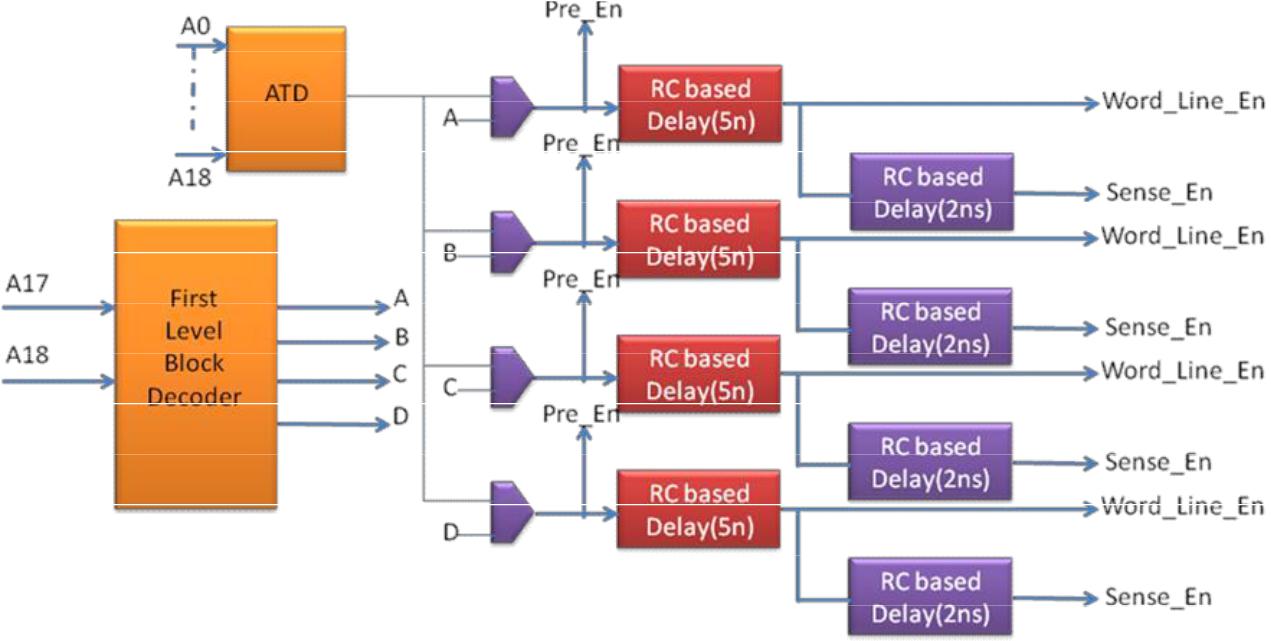
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **S.No** |  | **Inputs** |  | **Sources** |  |
|  | 1 |  | A0-A16 |  | Input buffers |  |
|  | 2 |  | CE |  | Input buffers |  |

1. GLC outputs

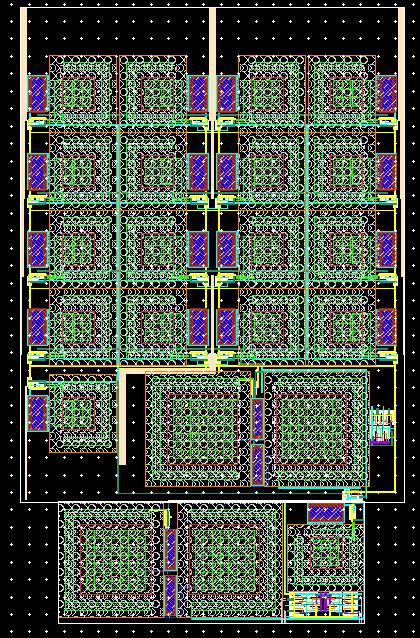
Table 15. GLC Outputs

|  |  |  |
| --- | --- | --- |
| **S.No** | **Outputs** | **Sinks** |
| 1 | Pre\_En(0:3) | Precharge Banks |
| 2 | Word\_Line\_En(0:3) | Row Decoder |
| 3 | Semse\_en(0:3) | Sense Amplifier |

1. Block Diagram

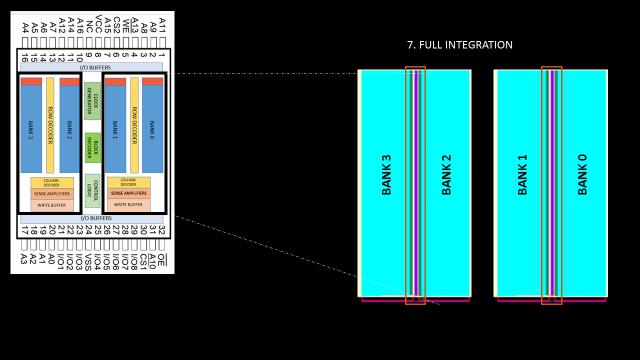


**Figure 54: Block diagram of Global level control circuit**

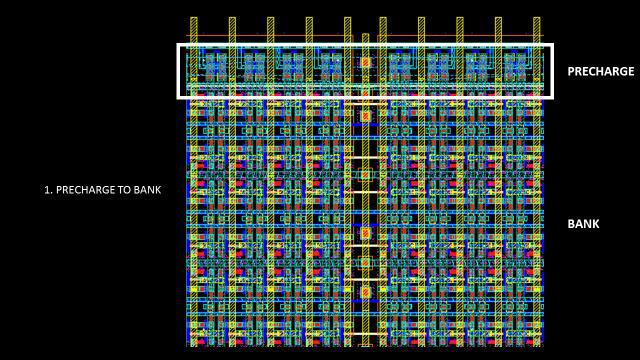


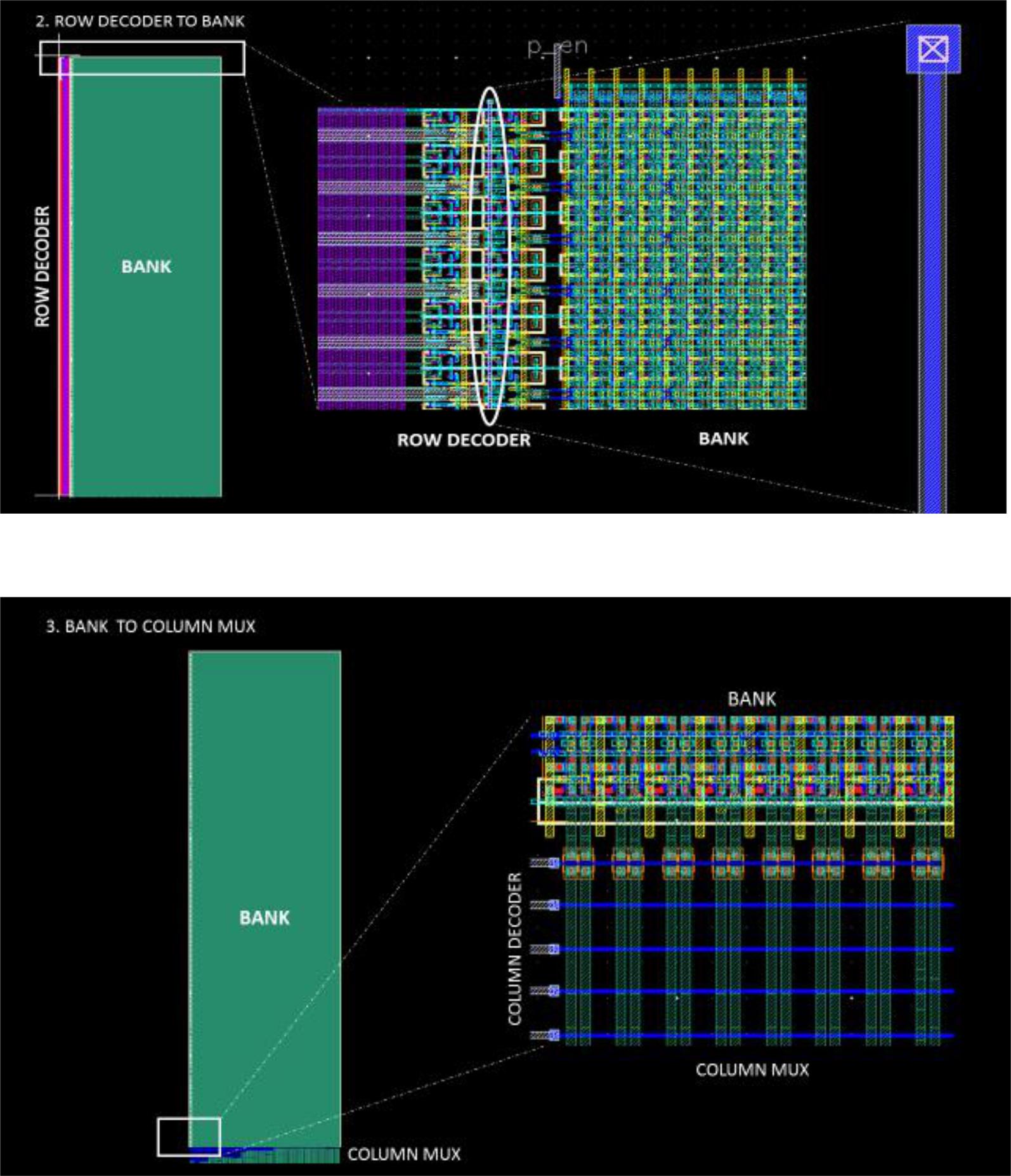
**Figure 55 : Full ATD module**

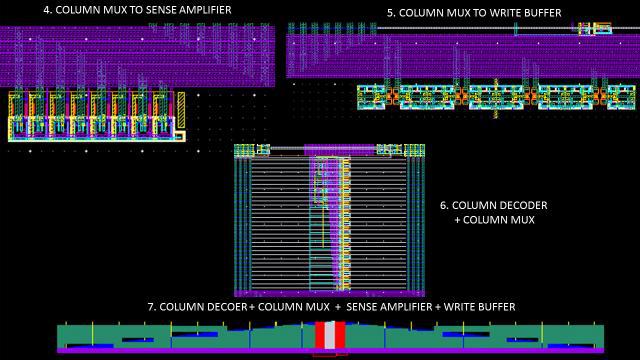
1. Integration
   1. Full chip layout integration
   2. FULL CHIP LAYOUT VIEW



**Figure 58:Integrated Memory Layout**







1. READ, WRITE OPERATION OF 1024\*16 SRAM CELL
2. Testing Procedure:

Simulation of write operation followed by read operation ensures that data is being written as well as read correctly. As there are 1024 rows in one column, bit line capacitance will be large. This simulation will ensure the proper working. As the word size of this memory is 8 bit we have simulated for 1024\*8 SRAM Cells integrating with precharge, colulmn mux, write drivers, sense amplifiers.

**Figure 65: Integration of 1024 \* 64 SRAM cell**



**Figure 66:- Different signals used for simulation**

* 1. Simulation Results:
* Voltage diff between BL and BL\_BAR after 3ns of WL active for Write operation(mV):-

630mV

After Word Line (WL) is active for writing zero, word line driver will discharge the BL or BL\_BAR depending on, where zero need to be written and other line will stay at precharged voltage level. 630mv of difference is created just 3ns after the WL activation, which is enough for write operation.

* Voltage difference between BL and BL\_BAR after 2ns of WL active for read operation (mV) :- 200mV

BL and BL\_BAR are precharged and Word Line (WL) is actived for reading the data in

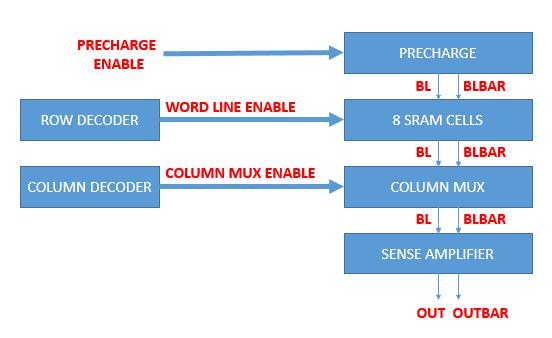
cell through access transistor, either BL or BL\_BAR will discharge through pull down

transistor, in accordance with the data stored in the cell and other line will stay at precharged voltage level. 200mv of difference is created just 2ns after the WL activation,

which is sufficient for sense amplifier to detect the data and give output accordingly.  RMS current considering one write and one read operation:- 78.4uA

1. CRITICAL PATH SIMULATION:

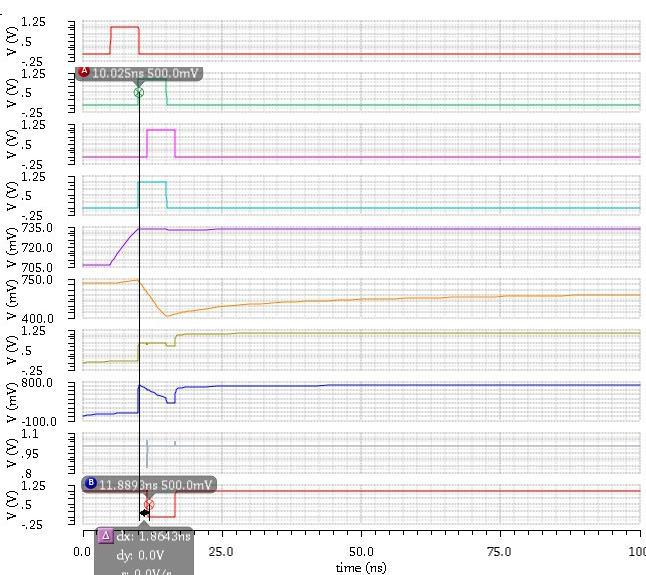
Critical Path Testing is finding the longest path in a project and analyzing it for correct functioning. Here is the path for critical testing



*Fig: Test bench for Critical Path Testing*

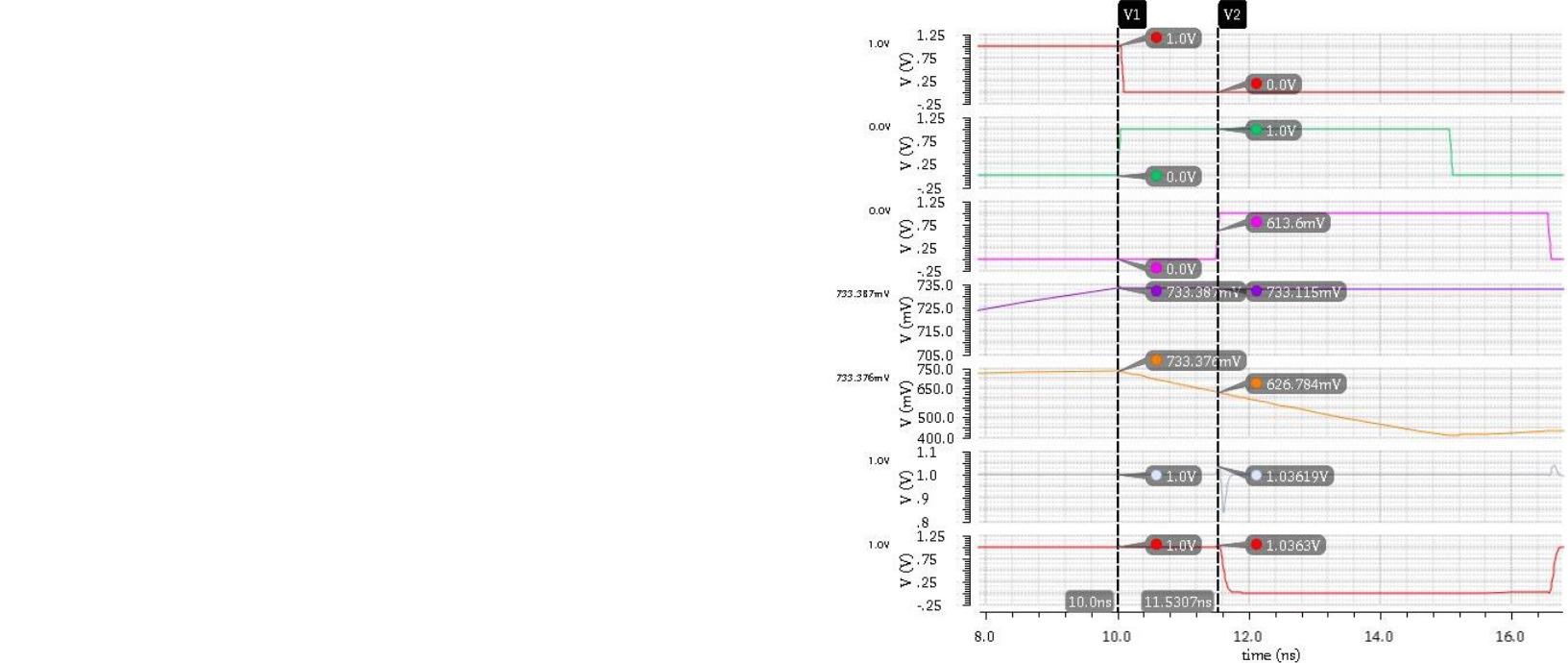
A number of simulations were carried out, waveforms are plotted and values were tabulated**.**

**a)** **READ**



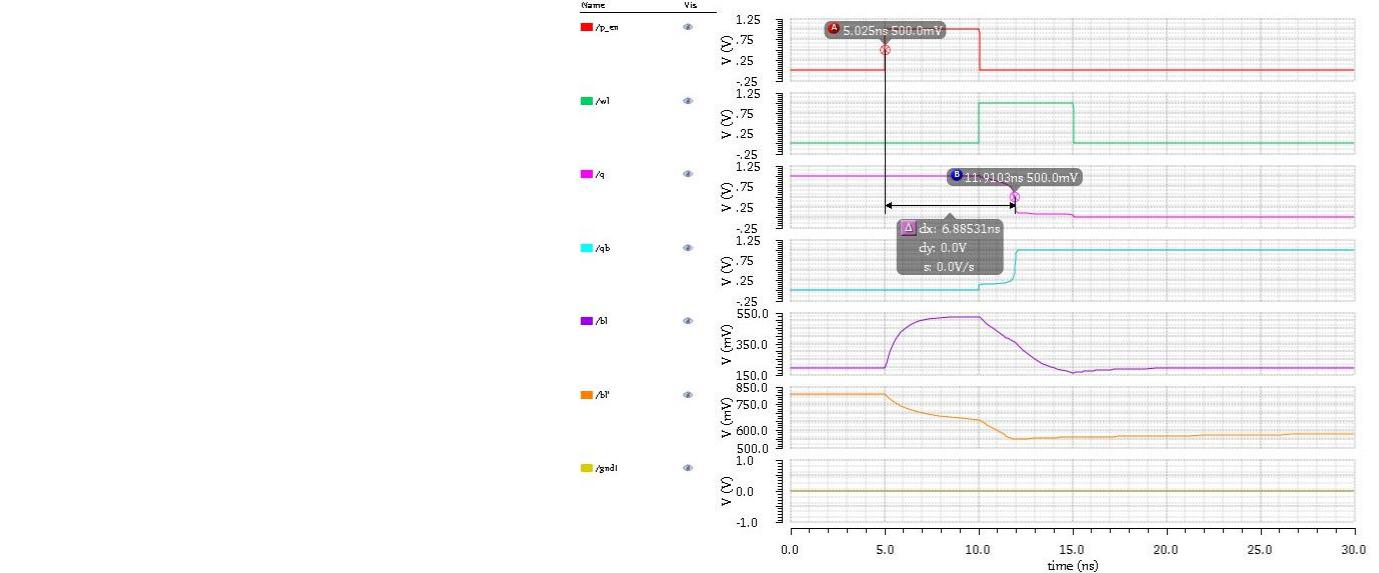
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **CORNER** |  | **DELAY (ns)** |  |  |  | **ACCESS (PRECHARGE** |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  | **(LVT, HVT, TEMP)** |  |  |  |  |  | **ENABLE TO DATA** |  |  |  |
|  |  |  |  |  |  |  |  | **OUT) (ns)** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | |  |  |  | | |  |  |  |
|  |  |  | |  |  |  |  | |  |  |  |
|  |  | **Typical Case** |  | **1.8643** |  |  |  | **6.9** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | |  |  |  |  | |  |  |  |
|  |  | **Best Case** |  | **1.55** |  |  |  | **6.55** |  |  |  |
|  |  | **ff, ff, -40** |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **Worst Case** |  | **11.8** |  |  |  | **6.783** |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  | **ss,ss,-40** |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

**READ VALUES**

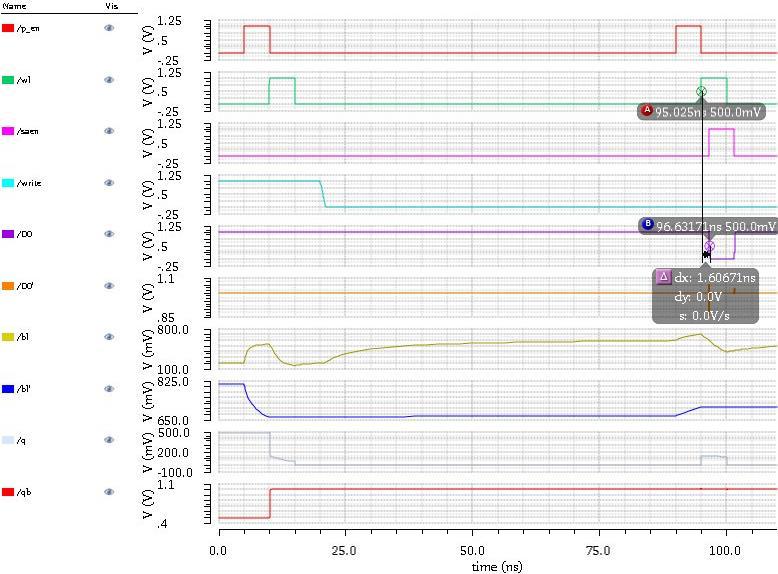


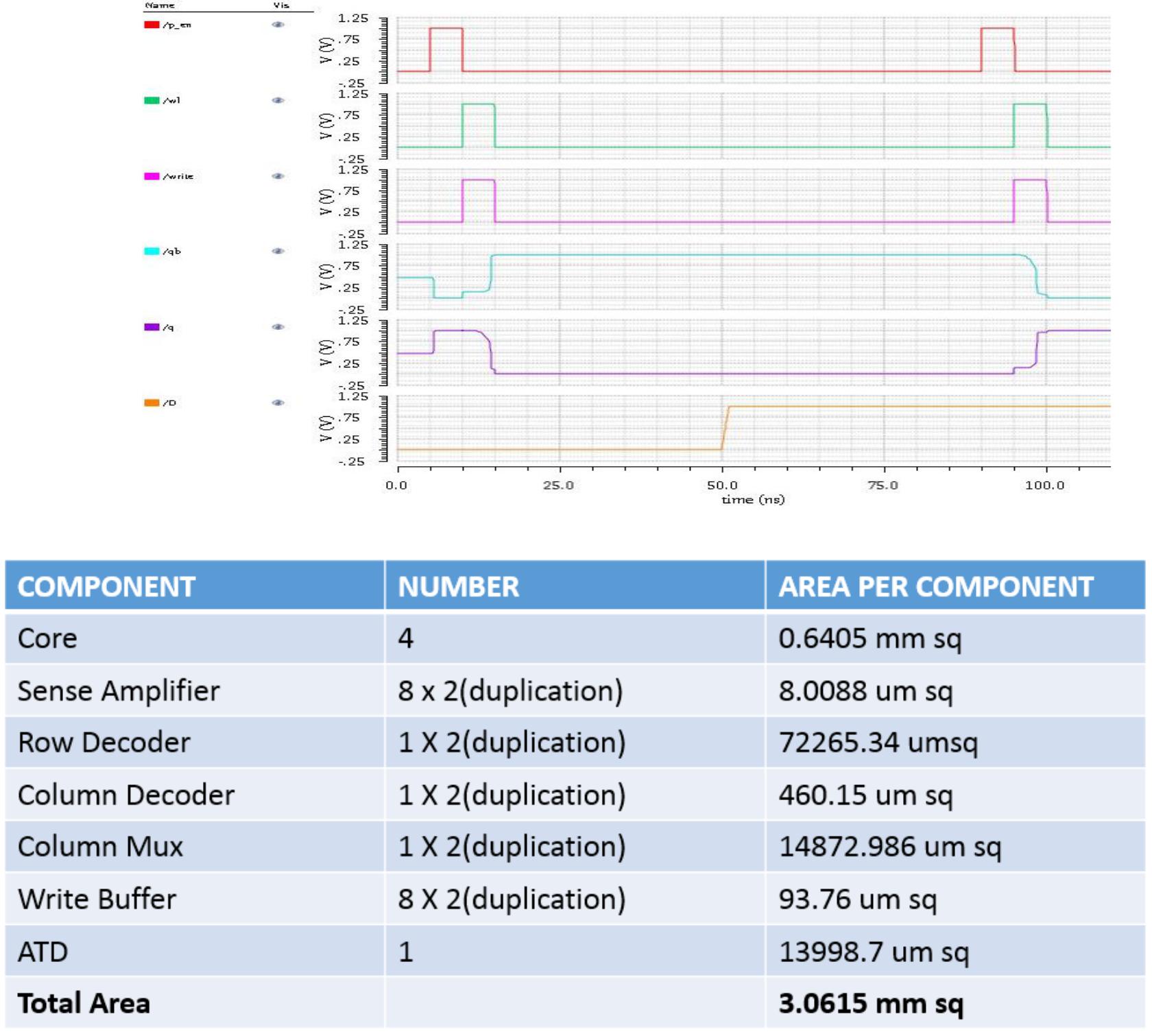
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **SIGNAL** |  |  |  | **VALUE AT** |  |  |  | **VALUE AFTER** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **10 nS** |  |  |  | **11.5 Ns** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | |  |  |  | |  |  |  | |  |  |
|  |  |  | |  |  |  | |  |  |  | |  |  |
|  |  | **BL** |  |  |  | **733.387 mV** |  |  |  | **733.115 mV** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | |  |  |  | |  |  |  | |  |  |
|  |  | **BLBAR** |  |  |  | **733.376 mV** |  |  |  | **626.784 mV** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **DIFFERENCE** |  |  |  | **0.011 mV** |  |  |  | **106.331 mV** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  | **BETWEEN BL AND** |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **BLBAR** |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**b) WRITE**



|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **CORNER** |  |  |  | **DELAY** |  |  |  | **ACCESS** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | **(ns)** |  |  |  | **(PRECHARGE** |  |  |  |
|  |  |  |  |  |  |  |  | **ENABLE TO DATA** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | **OUT) (ns)** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | |  | | |  |  | | |  |  |  |
|  |  | |  |  | |  |  |  | |  |  |  |
|  | **Typical Case** |  |  |  | **1.8853** |  |  |  | **6.88** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |





6 IOPADS and IO Buffers

IOPADS were added to the memory core to form the complete chip. There are 32 IOPADS corresponding to the 32 pins in the chip.

ESD(Electrostatic Discharge) Protection was provided using a pair of NMOS, PMOS connected as diodes. Whenever a very high voltage appears at pins, it biases the diodes and bypasses through it.

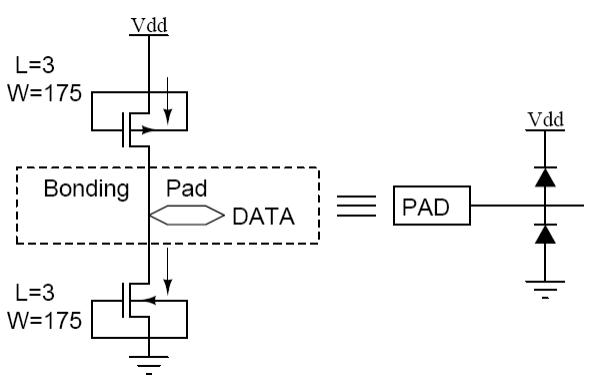
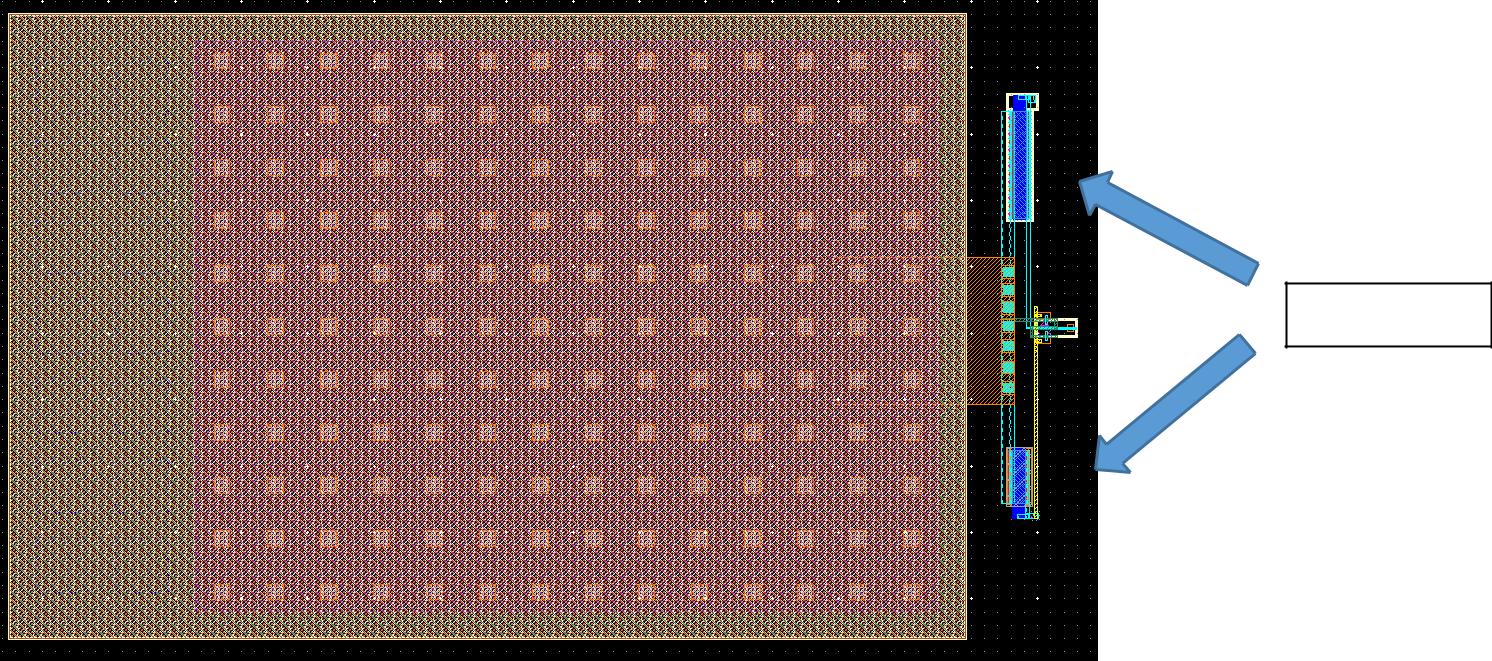


Figure :ESD diodes and IOPADS



ESD Diodes

Figure : Layout of IOPAD with ESD protection and input buffer

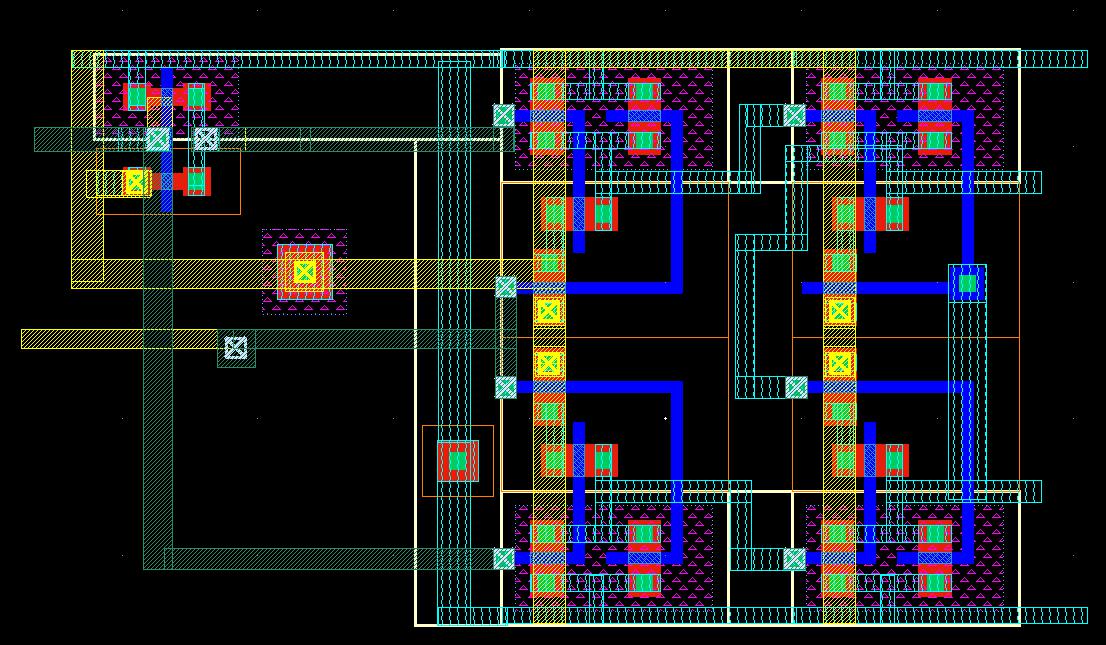


Figure : Layout of Output Buffer with Output Enable

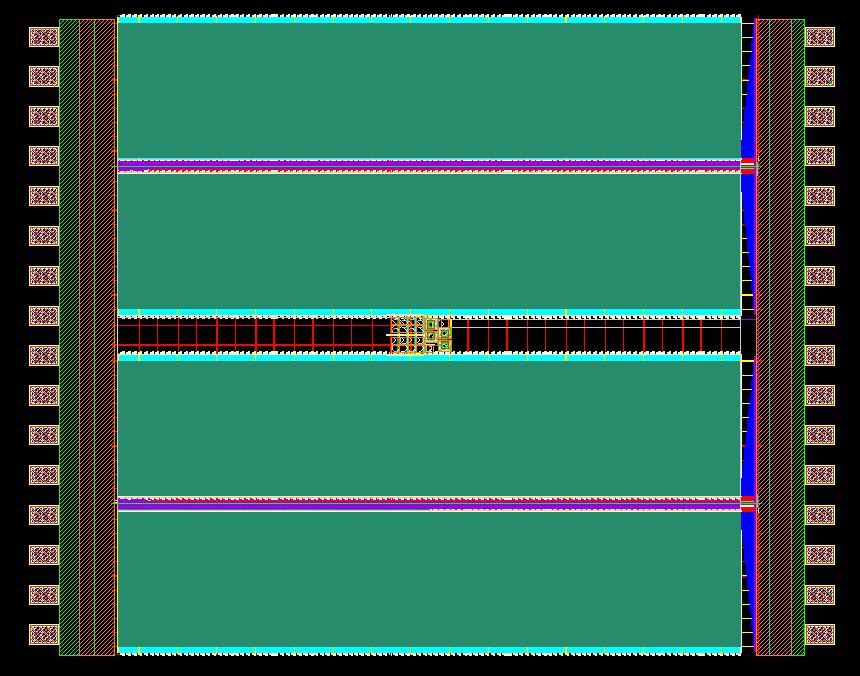


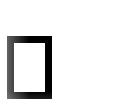
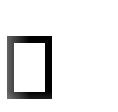
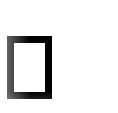
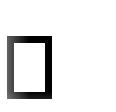
Figure : Layout of final chip with IOPADS and power rings

7 Salient Features

Almost all logic(especially decoders) is implemented using source coupled logic.

All word lines (and the block decoder line in divided word line)are strapped using METAL 1 to reduce poly resistance Twisting of bitlines is done for every 64 cells and this alternates over adjacent columns.

8 Conclusion and Future Work

* + SRAM design and simulation is complete. 
  + Integrated Simulation is run at 1 V and retention voltage 0.6. 
  + Layouts are LVS / DRC clean. Control circuit layout is not integrated with the core. 
  + Post Layout simulation for complete memory block is done with I/O pads 
    1. REFERENCES:

1. Evert Seevinck, Frans J. List and Jan Lohstroh, “Static Noise Margin Analysis of MOS SRAM Cells”,

IEEE Journal of Solid-state circuits”, vol – 22, No. 5, 1987.

1. Christiensen D.C.Arandilla, Anastacia B Alvarez “Static Noise Margin of 6T SRAM Cell in 90nm th

CMOS” 2011 UKSim 13 International Conference on Modelling and Simulation.

1. *A Low-power CMOS Thyristor Based Delay Element With Programmability Extensions by* Colin J.Ihrig and team (GLSVLSI-09).
2. Kiyoo Itoh, Katsuro Sasaki, Yoshinobu Nakagome, “Trends in Low- power RAM circuit Technologies”, Proceedings of the IEEE, vol. 83, No. 4, April 1995.
3. Evert Seevinck, Petrus J. van Beers and Hans Ontrop,”Current Mode Techniques for High Speed VLSI circuits with Application to Current Sense Amplifier for CMOS SRAM’s” IEEE journal of Solid

State circuits, vol 26, No. 4, April 1991.

1. J.M.Rabaey, A.Chandrakasan, B.Nikolic, “*Digital Integrated Circuits: A Design Perspective*”,

Prentice Hall

1. IBM Application Note “ Understanding Static SRAM Operation” 8. John F Wakerly, “Digital Design Principles and Practices”.

